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Characterization of Hot Electron Induced Interface States in LATID MOS Devices Using an Improved Charge Pumping Method

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This paper proposed an improved charge pumping method and a novel approach to characterize the spatial distribution of the interface states caused by the hot electron effect. A set of LATID (Large-Tilt-Angle Implanted Drain) MOS devices was studied to investigate the influence of source/drain implantation angle on the distribution of generated interface states. We found the generated interface state is the main cause of degradation and is closely related to the drain current reduction ($\Delta I_D/I_D$) in the linear region. Device with smaller implantation angle exhibits higher value of interface states. This improved approach turns out to be a successful way to analyze the hot carrier effect in different drain engineered devices.

1. Introduction

Interface state generation and oxide charge in the gate dielectric have been known as the fundamental long-term degradation mechanisms in submicron MOSFET's. The region degraded by hot carrier injection and the distribution of generated interface states will become significant when and if the degraded region becomes comparable with the channel length. The charge pumping technique[1-2] was proven to be a powerful method for characterizing the energy and spatial distribution of hot carrier generated interface states. The conventional methods[3-4] varied source and drain reverse bias to probe the depletion layer width at channel-drain junction to evaluate the lateral distribution of interface states. However, due to the limitation of the applied reverse bias , the delpetion width can not be increased any longer, so they could only provide a limited range of distribution around the gate edge near the drain.

Recently, LATID structure[5] in MOS device design has drawn much interest in terms of device design optimization and characterization. None has been reported regarding the interface state generation of such devices under hot carrier stress. In this paper, an improved approach to reliably characterize the spatial distribution of generated interface states (N_{it}) is first developed. A 2-D device simulator is used to verify the validity of the current approach. The influences of souce/drain implantation angles (θ) on the distribution of hot carrier induced interface states, the relationship between the amount of generated N_{it} and the device degradation will then be studied.

2. An Improved Charge Pumping Method

As shown in Fig.1, assume the n-MOS device being measured has laterally nonuniform distribution of flat-band voltage V_{fb} and threshold voltage V_{th}, a pulse waveform with fixed base level and varying high level (V_{gh}) is applied to the gate. Only interface states in the region ΔL can be filled by electrons and recombined by holes periodically and contribute to the charge pumping current (I_{CP}), where ΔL is the difference between $LC(_{gl})$ and $LC(V_{gh})$, $LC(V_{gl})$ and $LC(V_{gh})$ are the postion where local V_{fb} equals V_{gl} and local V_{th} equals V_{gh}, respectively. In this study, emission time during the pulse swings are held to be the same over the entire channel region by keeping rise time and fall time constant, such as 0.5μs, and the period is 1.0μs. In fresh devices, N_{it} and the emission time are uniform distributed along the channel, I_{CP} should be proportional to ΔL, therefore, the I_{CP} - V_{gh} relation is identical to that of ΔL-V_{gh}, as illustrated in Fig. 2. The Maximum I_{CP} corresponds to the middle of the channel and the minimum value (more near) corresponds to the gate edge in LDD or LDD-like devices. After hot carrier stressing, considerable amount of interface states will be nonuniformly generated in the drain side. If stress does not induce trapped charges in the oxide, the local threshold voltage distribution will remain the same shape as that of fresh devices. Therefore, in the charge pumping measurement, a given V_{gh} will activate the same length of interface states as in the fresh devices to form the pumped current, higher current indicates larger amount of interface states are generated in this region. In other words, the relation V_{gh}-x is unchanged by the hot carrier stress. Based on the analytical expression of the I_{CP} as function of the V_{gh} value in a fixed base level charge pumping experiment[6], we can exchange the relation of I_{CP} - V_{gh} of post-stressed devices with N_{it} - x (x=ΔL, evaluated from gate edge) using the formula listed in Table 1, in which, dV/dx are obtained directly from I_{CP}-V_{gh} (i.e., x - V_{gh}) graph of fresh devices, or numerical fitting rising portion of I_{CP}-V_{gh} graph with an appropriate mathematical expression and then differentiating it. By utilizing the relationship between V_{gh} and distance, this improved charge pumping method does not

need to calculate troublesome delpetion width and can characterize the interface states ranged from the gate edge to the middle of the channel. The understanding of the full range interface states in submicron devices is essential for hot carrier reliability predictions.

Fig. 3 shows the measured charge pumping current versus the input gate voltage, V_{gh}, for a device under various time stress. In this figure all curves are started at the same V_{gh} value, which gives the information that threshold voltage shift is negligible during the stress. Fig. 4 shows the time evolution of $\Delta N_{it}(x)$ distribution along the channel. Most of the generated interface states are located in the high electric field region, and the peak value is about at the junction between n^- region and channel region. The linear region drain current is greatly degraded by these states through reduing the amount of mobile charges and enhancing the surface scattering, this effect is verified by placing the $\Delta N_{it}(x)$ for 10^4 seconds stress on the interface of device simulator - Minimos4.1, Fig. 5 shows the simulation results, good matches can be achieved which justifies the validuty of the present method.

3. Investigation of the Hot Carrier Induced Interface States in LATID MOS Devices

A series of LATID MOS devices with gate oxide thickness of 140Å, n^- dosage of 2×10^{13} cm^{-2} with energy 80Kev and various tilt angle θ (0° to 60°) have been fabricated using the .7μm CMOS technology. By applying the above technique to characterize the interface states in stressed LATID devices, Fig. 6 shows the time evolution of $\Delta N_{it}(x)$ distribution along the channel in drain side for device with θ= 30°, in which the N_{it} is largely increased with increasing stress time. While, the peak value is almost located at the same position. The ΔN_{it} distribution for devices with various θ value is shown in Fig. 7, in which, the greater the θ valueis, less interface state is generated. Furthermore, device with smaller θ value has much wider ΔN_{it} distribution than those of larger angles. In addition to large amount of interface states generated near the poly-gate edge which may degrade the carrier mobility at this region, our devices also show significant linear region transconductance degradation at high V_{GS} bias, so the interface states within the spacer region can not be ignored in terms of performance degradation. Figs. 8 and 9 show the time evolution of generated interface states and the associated drain current degradation ($\Delta I_D/I_D$) in the linear region. After DC stress at V_{GS}=3.5V and V_{DS}=7V, devices exhibit negligible threshold shift. As a consequence, Figs. 8 and 9 reveal that the hot carrier generated interface state is the main cause of device degradation and it is closely realted to the $\Delta I_D/I_D$ in the linear region. LDD device (0° S/D implantaion) has the greatest degradation, while 60° implantaion has the minimum interface states generated. This has been justified by the effective electric field concept from our previous study[7], in which the effective electric field (E_{eff}) from measured substrate current (I_B) and drain current (I_D) can be determined experimentally. This field is the overall result of the 2-D electric field and contributes to the observed impact ionization rate $\alpha\cdot\exp(-\beta/E_{eff})$, in which α and β are the coefficients of surface impact ionization rate. Fig. 10 gives the bias dependent of E_{eff} in LATID devices and shows large angle tilt implantation device has smaller E_{eff}. It means that the LATID device surferrs smaller high field heating effect, accordingly, less interface states are generated. The drain current degradation is thus decreased. Combining E_{eff} with the above results of ΔN_{it} in various devices, E_{eff} can be regarded as a useful quantity to explain the amount of the generated hot carriers within devices.

In short, n^- implantation with tilt angle can suppress the hot carrier effect in submicron devices. Larger implantation angle results in less generated interface states. Effective electric field successfully explains the amount of generated interface states in different LATID devices.

4. Conclusion

In this paper, a novel approach for characterizing the spatial distribution of hot electron induced interface states in LATID MOS devices has been proposed. It was developed based on the combined fixed base level charge pumping method and a derived transformation between the charge pumping current and the spatial distance. The measured interface states distribution is verified by 2D device simulations which shows pretty good agreements. One major application of the present improved method is to explore the hot carrier generated interface states in LATID MOS devices. It is found that the n^- tilt angle implant affects the distribution of generated interface states and must be taken into account during the device design. We conclude that useful information about hot carrier behaviors and the design of a hot carrier resistant structure device can be better understood through the use of the currently developed improved charge pumping method.

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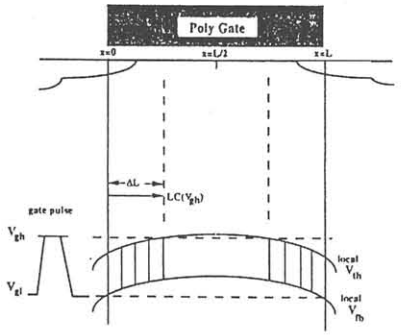

Fig. 1 Schematic diagram of the measurement method.

$$I_{CP} = k \int_{V_{gl}}^{V_{gh}} D_{it}(V)\, dV, \quad k = f \cdot q \cdot w, \qquad (1)$$

$$I_{CP} = k \int_{0}^{L} D_{it}(V) \frac{dV}{dx}\, dx, \qquad (2)$$

let $N_{it}(x) = D_{it}(V) \cdot \frac{dV}{dx}$, then

$$I_{CP} = k \int_{0}^{L} N_{it}(x)\, dx. \qquad (3)$$

$$\frac{dI_{CP}}{dv} = k\, D_{it}(V) = k \frac{N_{it}(x)}{\frac{dV}{dx}}, \qquad (4)$$

$$N_{it}(X) = \frac{1}{k} \frac{dI_{CP}}{dv} \frac{dv}{dx}, \quad x = \frac{L}{2} \cdot \frac{I_{CP}(V_{gh})}{I_{CP,max}}. \qquad (5)$$

Table 1 Formulae for evaluating $N_{it}(x)$ from measured I_{CP} - V_{gh} relationship.

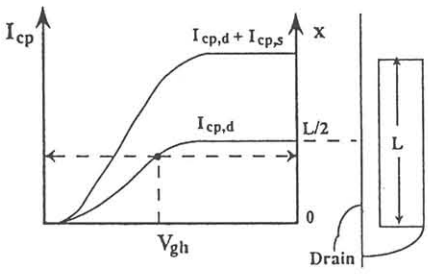

Fig. 2 The mapping relationship between I_{CP}-V_{gh} and V_{gh}-x for a fresh device.

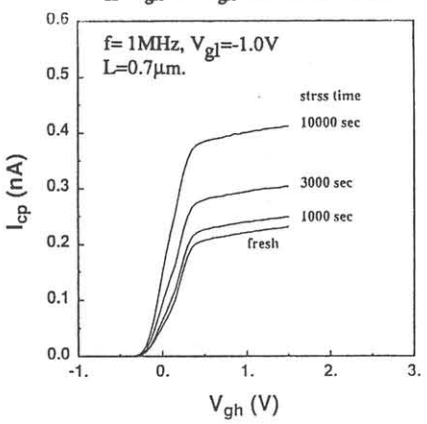

Fig. 3 Fixed base level charge pumping measurement of an LDD devices.

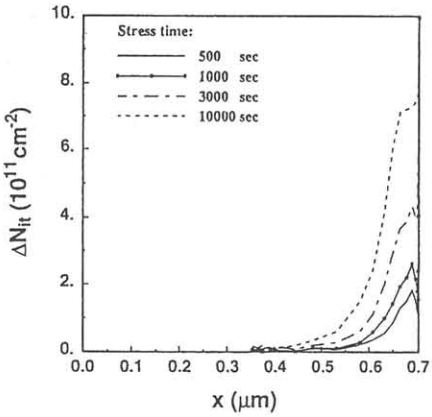

Fig. 4 Time evolution of ΔN_{it} distribution for a 0.7μm LDD device.

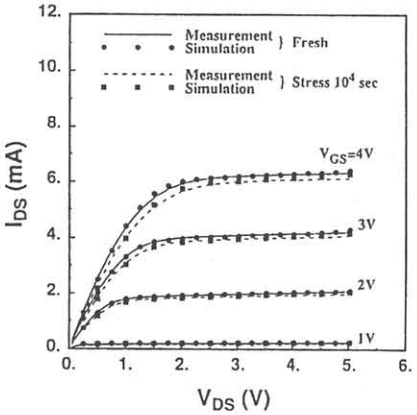

Fig. 5 The verification of the $\Delta N_{it}(x)$ by 2D simulation of the drain currents.

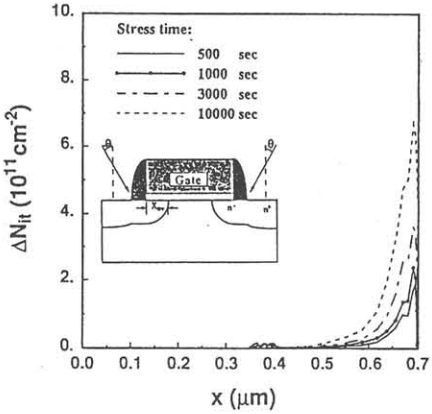

Fig. 6 Time evolution of ΔN_{it} distribution for a 0.7μm LATID device with θ= 30°.

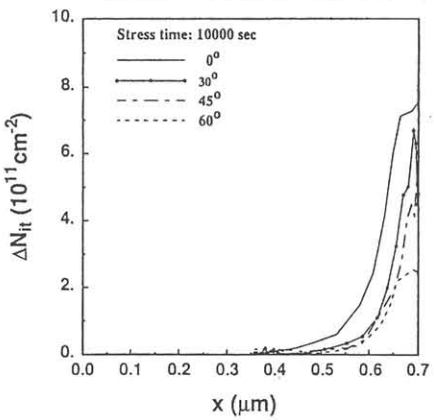

Fig. 7 The ΔN_{it} distribution for LATID devices with various θ values.

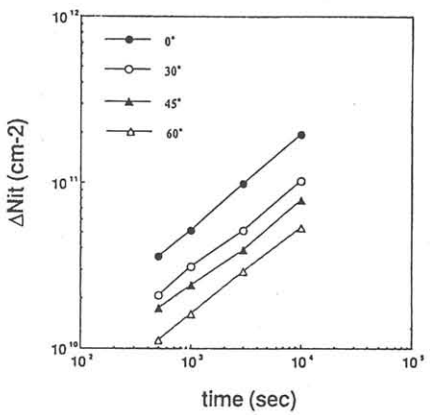

Fig. 8 Time evolution of total generated N_{it} for LATID devices with various θ values.

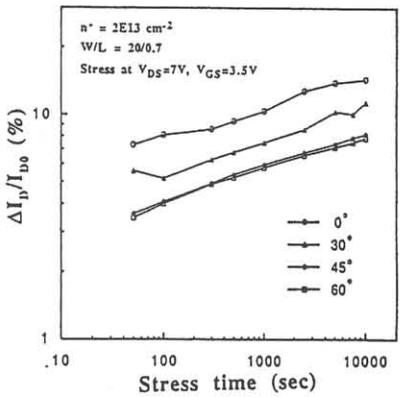

Fig. 9 Time evolution of drain current degradation for devices with various θ values.

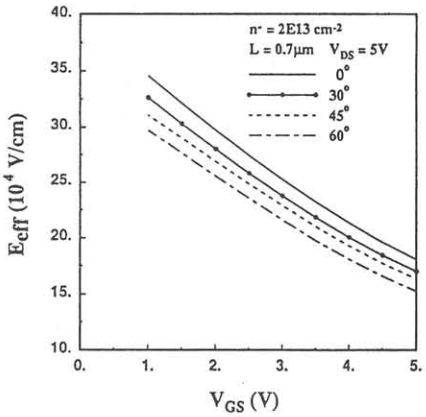

Fig. 10 Extracted effective electric field for various n^- implant angle.