A Two-Step Tunneling Model for the Stress Induced Leakage Current in Thin Silicon Dioxide Films

Naoki Yasuda, Nalin Patel* and Akira Toriumi

ULSI Research Labs, R&D Center, Toshiba Corporation 1, Komukai Toshiba-cho, Saiwai-ku, Kawasaki 210, Japan

The stress induced leakage current in thin silicon dioxide films is modeled with a two-step elastic tunneling process via an intermediate trapping site. The traps most efficient in producing the leakage current have an energy level of 2.0 eV below the conduction band of SiO₂. The dependences of the leakage current on the oxide thickness and voltage polarity $(t_{ox}: 5-7 \text{ nm})$ indicate the trap centroid located near the center of the oxide layer and an estimated trap distribution width of 1.4 nm. The current-voltage (I - V) characteristic of the leakage current calculated from the trap distribution shows a good agreement with the measured I - V curve.

1 Introduction

The stress induced leakage current in thin silicon dioxide films is a major limiting factor for scaling down the tunnel oxide of EEPROMs [1]. Several models have so far been proposed to explain the mechanism of the leakage current, which include electric field enhancement due to trapped positive charge [2], local barrier height lowering [3], and trap-assisted tunneling [4]. In recent reports, a close relation is pointed out between the stress induced leakage current and the traps generated during high-field stressing [4, 5]. In the present work, the authors examined quantitatively how a trap-assisted tunneling model can explain the properties of the stress induced leakage current.

2 Experimental Results

The dependences of the stress induced leakage current on the gate oxide thickness and gate voltage polarity were measured on metal-oxide-semiconductor (MOS) capacitors and transistors with a gate area of $0.01 - 0.15 \text{ mm}^2$. The gate oxides were prepared in dry O₂ at 800°C to thicknesses of 5.2 - 7.5 nm for the capacitors and 4.0, 6.5 nm for the transistors.

The stress induced leakage current measured for the capacitors with different oxide thicknesses is shown in Fig. 1, indicating a decrease in the leakage current as the gate oxide thickness increased. Figure 2 shows the voltage polarity dependence of the leakage current measured for the transistors ($t_{\rm ox} = 6.5 \,\mathrm{nm}$).

The stress induced leakage current was larger in reverse bias (i.e., opposite polarity to that of high-field stressing) than in forward bias. On the other hand, no voltage polarity dependence was observed for the transistors with a thin gate oxide ($t_{\rm ox} = 4$ nm).

3 Model

The authors propose a two-step tunneling process via an intermediate trapping site as the mechanism of the stress induced leakage current. In this model,



Figure 1: Oxide thickness dependence of stress induced leakage current. Stress condition: 11 MV/cm, 100 s. \bigcirc : measured at 6 MV/cm. Solid curve: calculated for $A = 5 \times 10^{-3} \text{ nm}^{-1}$ and D = 0.7 nm.

^{*} Present address: Toshiba Cambridge Research Center, GB



Figure 2: Voltage polarity dependence of stress induced leakage current. Dashed curve: reverse leakage current (i.e., measured in the opposite voltage polarity to that of high-field stressing). Dotted curve: forward leakage current.

electrons elastically tunnel into an intermediate trap and then tunnel out to the conduction band of SiO₂ in a high field, or to the anode electrode in a low field. The electron current flowing into the intermediate trap, J_1 , and that flowing out of the trap, J_2 , are expressed as

$$J_1 = q N_{\rm ox} (1 - f) / \tau_1 \tag{1}$$

$$J_2 = q N_{\text{ox}} f / \tau_2, \qquad (2)$$

respectively, where q is the electronic charge, N_{ox} is the density of the traps at $x = x_{elas}$, f is the occupation probability of the traps, and τ_1 , τ_2 are tunneling time constants (See Fig. 3). The location of the intermediate traps, x_{elas} , is expressed as

$$x_{\rm elas} = (E_{\rm b} - E_{\rm trap})/E_{\rm ox} \tag{3}$$

where $E_{\rm b}$ is the barrier height at the Si/SiO₂ interface (3.0 eV), E_{trap} is the trap energy level with respect to the conduction band of SiO_2 , and E_{ox} is the electric field in the oxide. The tunneling time constants are calculated on the basis of Wentzel-Kramers-Brillouin (WKB) approximation, resulting in

$$\frac{1}{\tau_{1}} = \sigma v_{t} N_{c} \exp\left\{-\beta (E_{b}^{3/2} - E_{trap}^{3/2})/E_{ox}\right\}$$
(4)

$$\frac{1}{T_2} = \sigma v_t N_c \exp\left\{-\beta (E_{\rm trap}^{3/2} - E_{\rm a}^{3/2})/E_{\rm ox}\right\}$$
(5)

where σ is the capture cross section of the traps, v_t is the thermal velocity of electrons, N_c is the effective density of states in the silicon conduction band, β is defined as $\beta = 4\sqrt{2m^*q}/3\hbar$ with $m^* = 0.5m_0$ [6], and E_{a} is the effective anode barrier height defined as $E_{\rm a} = E_{\rm b} - E_{\rm ox} t_{\rm ox}$ for a low field $(E_{\rm ox} t_{\rm ox} \le E_{\rm b})$ and $E_{\rm a} = 0$ for a high field $(E_{\rm ox} t_{\rm ox} > E_{\rm b})$. The stress induced leakage current is expressed as

$$J = J_1 = J_2 = q N_{\rm ox} / (\tau_1 + \tau_2), \tag{6}$$



Figure 3: Two-step tunneling model. Electrons injected from the cathode elastically pass through the oxide via an intermediate trapping site generated during high-field stressing.

since it is a steady-state tunneling current through the intermediate traps.

For a given trap distribution, the stress induced leakage current is maximal for minimum $(\tau_1 + \tau_2)$. This condition is given by $\tau_1 = \tau_2$. Equations (4) and (5) indicate that $E_{\text{trap}} = (1/2)^{2/3} E_{\text{b}} (= 2.0 \text{ eV})$ gives $\tau_1 = \tau_2$ in the high field region ($E_{\text{a}} = 0$ for $E_{\text{ox}} > E_{\text{b}}/t_{\text{ox}}$). This means that the traps with an energy level of 2.0 eV below the conduction band of SiO₂ are most efficient in producing the stress induced leakage current in the high field region.

Spatial 4 Distribution of Traps

The spatial distribution of the 2.0 eV traps is estimated from the stress induced leakage current measured in a high field region ($E_{ox} = 6 \text{ MV}/\text{cm}, t_{ox} = 5.2$ - 7.5 nm). A Gaussian distribution is assumed for the trap density,

$$N_{\rm ox}(x) = N_{\rm t} \exp\left\{-\frac{(x-x_0)^2}{D^2}\right\},$$
 (7)

where $N_{\rm t}$ is the maximum trap density, $x_0 ~(\approx t_{\rm ox}/2)$ is the trap centroid, and D is the half width of the trap distribution. To a first approximation, N_t and D are assumed to be constant regardless of the oxide thickness. The dependence of the trap centroid on the oxide thickness is introduced as

$$x_0 = \frac{t_{\rm ox}}{2} \, \left(1 + A t_{\rm ox} \right),$$
 (8)

which gives a symmetric trap distribution for thin oxides and a shift in the trap centroid towards the anode for thick oxides. The voltage polarity dependence of the stress induced leakage current is explained by this



DISTANCE FROM CATHODE

Figure 4: Model for polarity dependence of stress induced leakage current. The traps at x_{elas} and $t_{ox} - x_{elas}$ generate the leakage current in forward and reverse bias, respectively. The reverse current is larger than the forward current when the trap centroid is shifted towards the anode.

shift of the trap centroid, causing a larger trap density at $x = t_{ox} - x_{elas}$ than at $x = x_{elas}$ (Fig. 4). From Eqs. (7) and (8), the ratio between the reverse

From Eqs. (7) and (8), the ratio between the reverse leakage current J_{rev} and the forward leakage current J_{for} is expressed as

$$J_{\rm rev}/J_{\rm for} = \exp\left\{At_{\rm ox}^2(t_{\rm ox} - 2x_{\rm elas})/D^2\right\}.$$
 (9)

The measured leakage currents at $E_{\rm ox} = 6 \,\mathrm{MV/cm}$ in Fig. 2 give $A/D^2 = 0.01$. Using this relation, the half width of the trap distribution is found to be D = $0.7 \,\mathrm{nm}$ (Fig. 1). The parameter A is then obtained as $A = 5 \times 10^{-3} \,\mathrm{nm^{-1}}$, which indicates a very small deviation in the trap centroid from the center of the oxide with $\Delta x_0/(t_{\rm ox}/2) = 3\%$ for $t_{\rm ox} = 6.5 \,\mathrm{nm}$.

Thus, the traps responsible for the stress induced leakage current in the high field region (i.e., 2.0 eV traps) are considered to be located near the center of the oxide. The full width of the trap distribution is estimated to be 1.4 nm for $t_{\rm ox} = 5 - 7$ nm.

5 Current-Voltage Characteristic

The current-voltage characteristic of stress induced leakage current was calculated with the estimated spatial distribution of the 2.0 eV traps, and compared with the measured I - V characteristic (Fig. 5). The calculated I - V curve was in good agreement with the measured leakage current in the high field region $(E_{\rm ox} > E_{\rm b}/t_{\rm ox})$ where the contribution of the 2.0 eV traps to the leakage current was predominant. The discrepancy observed in the low field region is considered to be due to traps deeper than 2.0 eV, whose contribution becomes significant in the low field region.



Figure 5: I-V characteristic of stress induced leakage current for $t_{ox} = 5.2 \text{ nm}$. \blacksquare : measured after high-field stressing of 11 MV/cm, 100 s. Dashed curve: calculated for the distribution of 2.0 eV traps.

6 Conclusions

The stress induced leakage current in thin silicon dioxide films ($t_{ox} = 5 - 7 \text{ nm}$) has been modeled with a two-step tunneling process via an intermediate electron trap. The traps most efficient in producing the leakage current in the high field region ($E_{ox} > E_b/t_{ox}$) are those with an energy level of 2.0 eV below the conduction band of SiO₂. The centroid of the 2.0 eV traps is located near the center of the oxide, with their estimated distribution width of 1.4 nm. The I - Vcharacteristic of the leakage current in the high field region is well reproduced by using the trap distribution.

References

- K. Naruke, S. Taguchi and M. Wada, *IEDM Tech. Dig.*, p. 424 (1988).
- [2] J. Maserjian and N. Zamani, J. Vac. Sci. Technol. 20, 743 (1982).
- [3] P. Olivo, T. N. Nguyen and B. Riccó, IEEE Trans. Electron Devices 35, 2259 (1988).
- [4] R. Moazzami and C. Hu, *IEDM Tech. Dig.* p. 139 (1992).
- [5] R. Rofan and C. Hu, IEEE Electron Device Lett. 12, 632 (1991).
- [6] Z. A. Weinberg, J. Appl. Phys. 53, 5052 (1982).