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Numerical Simulation of Tunnel Effect Transistors Employing Internal Field Emission of Schottky Barrier Junction

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The tunnel transistor employing internal field emission of Schottky barrier junction (SBTT) is a promising element device for high-density and low-cost integration. In order to characterize the performance of SBTT, we have carried out 2-D numerical simulation on typical four types of device structures. When the channel layer is thicker than the depletion width near the drain formed by gate bias, the output characteristic of SBTT is triode-like. In the case of thin channel layer, the saturation feature appears due to pinch-off effect. A prototype n-channel SBTT of crystalline silicon has been fabricated and the transistor action is confirmed.

1. Introduction

A new type of tunnel-effect transistors employing internal field emission of Schottky barrier junction, Schottky barrier tunnel transistor (SBTT), was previously proposed[1]. The advantage of this device is simplified fabrication process due to elimination of the process for n^+ or p^+ islands for source and drain in addition to the unique operating principle with inherent high transconductance. Application of SBTT to TFT for active matrix LCDs is expected. Other important features are high-speed and small size, being useful to advance high integration of memories.

In this paper we show some results of 2-D numerical computer simulation on SBTT and discuss the distinct . An example of prototype device with a simple structure is also reported.

2. Fundamental Structure and Operating Principle

The fundamental structure of SBTT is apparently the same as conventional MOSFET or TFT which are composed of an insulated gate and a channel layer with source and drain contacts as shown in Fig.1(a). However, there are substantial differences between two: (i) the source contact of SBTT forms Schottky barrier to the channel layer instead of ohmic contact to highly doped island in conventional MOSFET. (ii) the channel layer is moderately doped to about 10^{17} cm^{-3}. Because of these two unique features, the proposed structure gives remarkable advantages in fabrication process. Processes for fabricating low resistivity islands for ohmic source and drain contacts can be unnecessary. Moreover, the moderately doped channel layer of SBTT can be free from short-channel effect because of narrow depletion-width at source and drain junctions. SBTT, therefore, has a great advantage with respect to down-sizing of device dimensions.

The operating principle of SBTT is entirely different from that of conventional FET. Figure 1(b) shows the energy-band diagram of the structure of Fig.1(a), when a positive drain voltage is applied. At zero gate bias, electrons can not be injected from the source electrode into the channel region because of the reverse direction of Schottky barrier at the source contact. When a sufficient positive gate bias is applied, the electric field of Schottky barrier junction close to the gate insulator is satisfactorily enhanced and thus electrons are emitted into the channel layer through Schottky barrier by tunnel-effect. SBTT is expected to have a high transconductance, because the tunneling current through Schottky barrier is sensitive to the electric

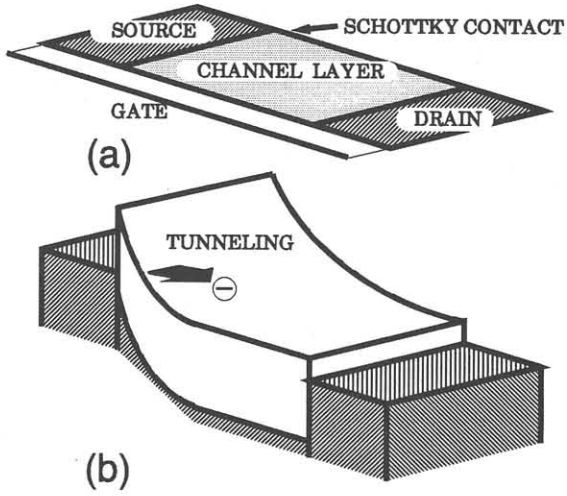

Fig.1 (a) Fundamental structure of SBTT and (b) energy band diagram when positive drain bias is applied. Tunneling current is controlled by gate bias.

field of the Schottky barrier modified by gate voltage. Furthermore, the device can operate fast, if the channel length is shortened.

Several types of transistors with Schottky barrier contact for source and drain have been proposed so far[2-4]. However, the operating principle of SBTT is entirely different from that of these transistors which work basically same as conventional FETs and the surface inversion layer (channel) is controlled by gate voltage. In contrast, in our devices the channel layer is structured from the first by a low-resistivity material.

3. Numerical Simulation on Various Device Structures

In order to evaluate the device characteristics and to design the optimized device structures, we have carried out 2-D numerical device simulation on typical four types of device structures shown in Fig.2. It was assumed in the present simulation that the channel layer material is n-type crystalline silicon. However, the basic idea of SBTT can be applied to other semiconductor materials such as amorphous silicon, polysilicon and other semiconductors. Yamaguchi model[5] was used to estimate the electron mobility. Since SBTT is principally a unipolar device, only the electron current are taken into account. The details of simulation method was stated in a previous paper[1]. For all structures in Fig.2 the Schottky barrier height, the channel length and the oxide thickness were reasonably assumed to be 0.7 eV, 500 nm, 50 nm, respectively. The width of channel layer was 1 μm. The donor densities of the channel region were 10^{17} cm^{-3} for Type-I and II, and 5×10^{16} cm^{-3} for Type-III and IV.

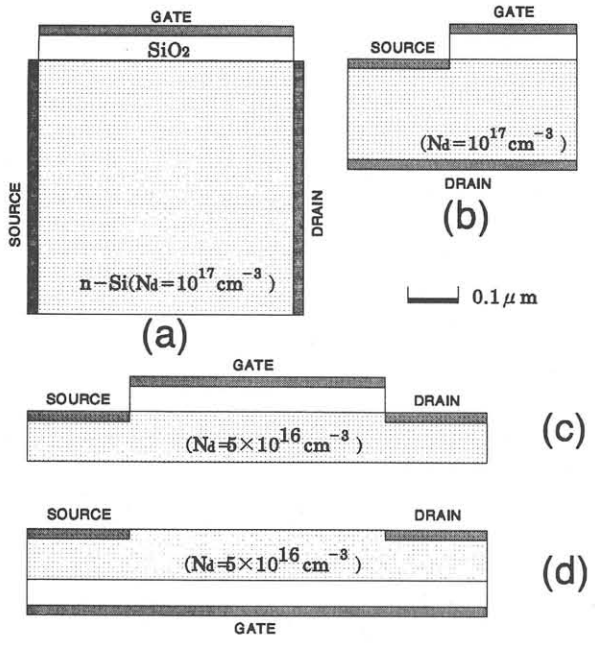

Fig.2 Four types of device configuration used device simulation. (a)Type-I:basic structure, (b)Type-II:vertical structure, (c)Type-III:coplanar structure and (d)Type-IV:staggered structure.

Type-I of Fig.2 is a basic and simplest structure with Schottky contacts both at source and drain for simplicity of fabrication process, which can be realized using trenched source and drain electrodes. The channel thickness was chosen to be 500 nm. The Neumann free boundary condition was assumed at the bottom of the channel layer, which means that the material under the channel is insulator or p-Si. This structure is compatible with LSI planar technology.

Type-II is a vertical structure. In this structure the thickness of the channel layer, assumed here to be 200 nm, corresponds rightly to the channel length, so that the operation speed can be improved, because the channel length is easily reduced without limitation of the lithography process. The drain contact of Type-II was assumed to ohmic contact.

Type-III and IV have a planar structure and are so-called coplanar and staggered structures, respectively. These structures are appropriate to application to TFT for active matrix LCDs.

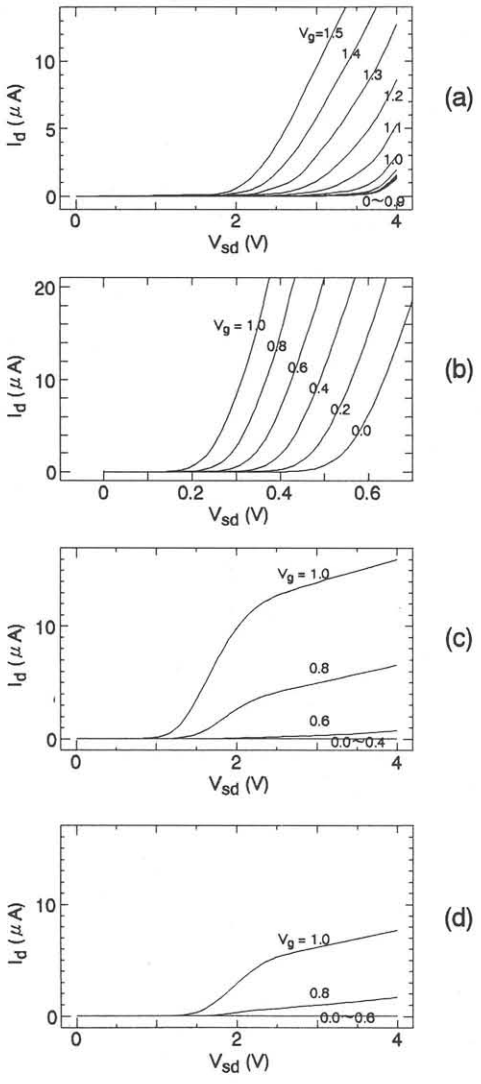

Fig.3 The output characteristics of different structures. (a) Type-I, (b) Type-II, (c) Type-III and (d) Type-IV.

Figure 3(a) shows the simulated output characteristic for Type-I structure. It is found that the output characteristic is distinctly different from those of conventional FET's. The drain current increases exponentially with increasing drain voltage showing nonsaturating "triode-like" feature. This is because in this structure the drain current is controlled only by the tunneling emission through source Schottky barrier. It is also seen that the increase in the drain current is not linear to the gate voltage. This nonlinear transconductance behavior may allow potential applications of this device to nonlinear analog circuits. Similar characteristic has also been found in SIT (static induction transistor)[6], PBT (permeable base transistor)[7] and triode-like JFET (junction-gate field-effect transistor)[8].

Type-II structure shows also nonsaturating "triode-like" characteristic as shown in Fig.3(b). Because of the ohmic drain contact and a short distance between source and drain, the threshold drain voltage is reduced in comparison with that of Type-I. This "triode-like" output is more favorable for applications to low-resistance load direct-drive circuits, because of their low output impedance and small distortion of I_d-V_g relationship.

On the other hand, the tendency of the drain current saturation is found for Type-III and IV planar structure devices as seen in Figs. 3(c) and (d). This tendency is because the thin channel layer near the drain is thoroughly depleted due to the potential difference between gate and drain. This is effective in reducing the leakage current which is a serious problem of conventional TFTs in LCDs, because the voltage difference between gate and drain is largest in the off-state. Even in the case of Type-I, if the channel layer gets thinner the saturation feature will be merged.

4. Example of Practical Device Operation

In this section only prototype of SBTT are exemplified. Other various modifications might be considered.

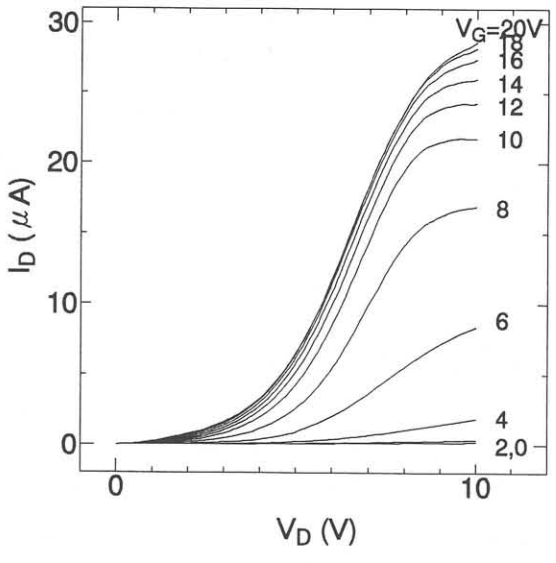

Fig.4 Experimental result of output characteristics from n-channel SBTT fabricated with crystalline silicon.

A prototype vertical device corresponding to Type-II in Fig. 2(b) was fabricated in order to confirm the proposed transistor action of SBTT. An n layer (10 Ωcm) epitaxially grow on 0.01 Ωcm) substrate was used as the channel. The thickness of the thermal oxide layer was 700 nm. The drain electrode was placed on the back side of the substrate. Schottky barrier junction at the source was formed by Pd/n-Si contact. Figure 5 shows the output characteristic at room temperature. The triode-like transistor action is obvious. The drain current increases exponentially with increasing drain voltage. As mentioned in the previous section, a nonsaturating future is essential in this configuration, because pinch-off effect does not occur. A weak saturation tendency in high drain current region is due to series resistance. The problems such as high threshold voltage and high driving voltage will be easily solved by optimizing doping concentration and device dimensions.

5. Summary

Promising characteristics of SBTT have been described on the basis of numerical simulation. In the case of thick channel layer the output characteristic of SBTT is triode-like and promising for analog circuits and high speed device applications. When the channel layer is as thin as the depletion width near the drain formed by gate bias, a saturation feature appears due to pinch-off effect. This effect is convenient to reduce the leak current in the off-state. We have fabricated a prototype n-channel vertical SBTT and its transistor action.

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