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Device Simulation with Quasi Three-Dimensional Temperature Analysis for Short Channel Poly-Si TFT

Tamio SHIMATANI, Takuji MATSUMOTO, Takeshi HASHIMOTO,
Noriji KATO*, So YAMADA* and Mitsumasa KOYANAGI

Research Center for Integrated Systems, Hiroshima University
1-4-2 Kagamiyama, Higashi-Hiroshima 724, Japan
* Fuji Xerox Co.

A new poly-Si TFT device simulator with quasi three-dimensional temperature analysis has been developed. In this simulator, the influences of the grain boundaries are incorporated into the mobility model when the basic semiconductor equations are solved. Furthermore, we have taken into account the self heating effect owing to a small thermal conductivity of the insulating substrate using quasi three-dimensional temperature analysis. We could accurately analyse the the temperature rise effect and the avalanche short channel effect in the short channel poly-Si TFT.

1. Introduction

Poly-Si TETs have been intensively investigated for the large area electronics applications such as active matrix LCD or page width image sensors. However, the operation mechanism of poly-Si TFT is very complicated and is not still fully understood because the poly-Si TFT includes many grain boundaries inside the device and the poly-Si substrate is floating. The floating substrate causes the accumulation of holes in n-channel TFT which are generated by the impact ionization around the drain. These holes causes the avalanche induced short channel effect[1]. In addition, the insulating substrate with a small thermal conductivity causes the serious self heating. The self heating becomes more serious as the channel length is reduced since the drain current increases[2]. It is very useful for understanding the operation mechanism of the poly-Si TFT in detail to employ the poly-Si TFT device simulator which can analyse these effects. However, works about such device simulator have been hardly reported so far. Then, we have developed a new poly-Si TFT device simulator with quasi three-dimensional temperature analysis in order to analyse these self heating effect and avalanche induced short channel effect.

2. Simulation Algorithm

The simulation flow chart is shown in Fig.1. It is very important in poly-Si TFT simulator how to take into account the influences of the grain boundaries. In our simulator, the influences of the grain boundaries are incorporated into the mobility model. The mobility is derived based on the model where it is assumed that the potential barrier is formed at the grain boundary and the carriers are transported over this potential barrier due to the thermionic emission mechanism[3)-5)]. The influences of the grain boundary trap density, trap level and grain size etc. can be described using this mobility

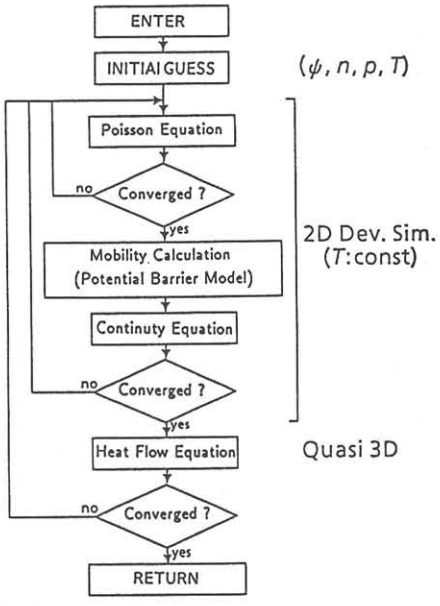


Fig.1 Simulation flow chart.

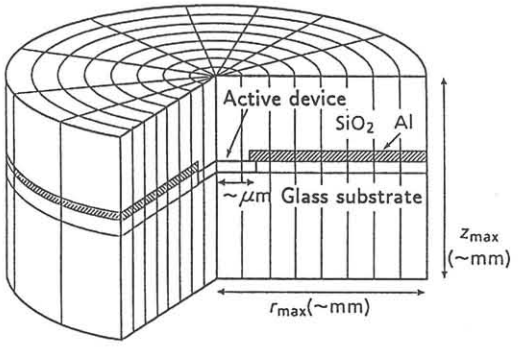


Fig.2 Mesh structure.

model. After solving the poisson equation and the current continuity equation, the power dissipation is calculated. This dissipation power is used when the heat flow equations are solved to obtain the temperature rise in the channel region. The heat flow equation should be solved in the wide region and in three-dimensional directions. However, it consumes a very long computational time. Then, we employ a new quasi three-dimensional temperature analysis where the cylindrical coordinates are adopted for describing the radial heat flow and reducing the computational turn-around time as shown in Fig.2. The doughnut meshes are used in the poly-Si film and the insulating substrate regions while the sector meshes are employed in the electrode regions. The device region is approximated by one small disk mesh which is placed in the center of the cylindrical coordinates. The dissipation power previously obtained is put into this small disk mesh when the heat flow equations are solved to obtain the device temperature. This temperature obtained is again used for solving device equations. We can obtain the device temperature in the steady state by repeating this procedure.

3. Results and Discussions

The threshold voltage vs. gate length relation and the subthreshold characteristics calculated by our simulator are shown in Figs.3 and 4. The threshold voltage is rolled off at the gate length less than 10μm due to the avalanche induced short channel effect but not due to the conventional short channel effect based on the charge share mechanism. In addition, the subthreshold swing is decreased as the gate length is reduced. This is different from the conventional short channel effect. It is clearly seen in the two dimensional distribution of hole concentration shown in Fig.5 that the short channel effect is caused by the impact ionization. As is clear in the figure, many holes generated by the impact ionization are accumulated in the poly-Si substrate near the source in

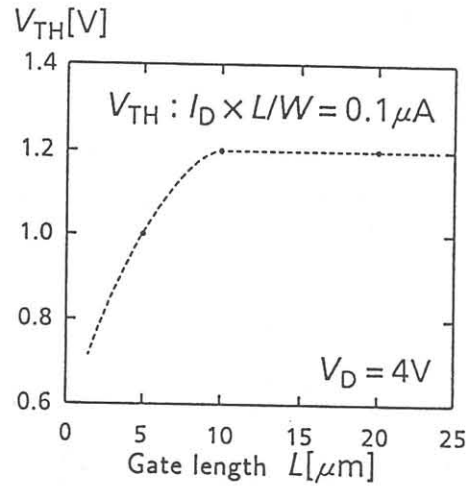


Fig.3 Gate length dependence of threshold voltage.

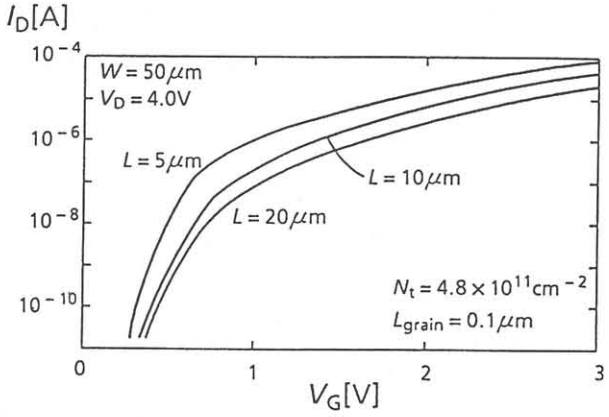


Fig.4 Subthreshold characteristics.

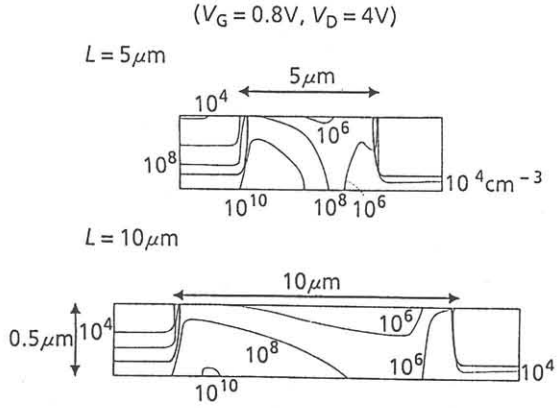


Fig.5 Two dimensional distribution of hole concentration.

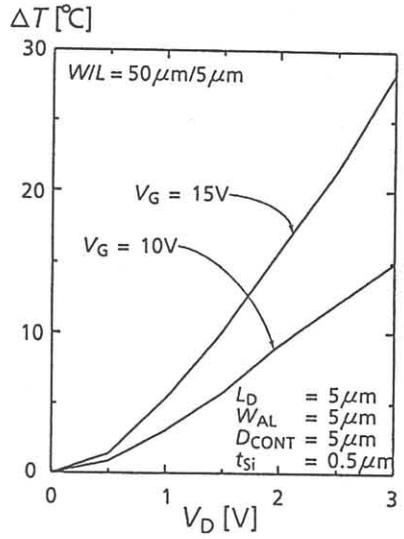


Fig.6 Temperature rise with increasing the drain voltage.

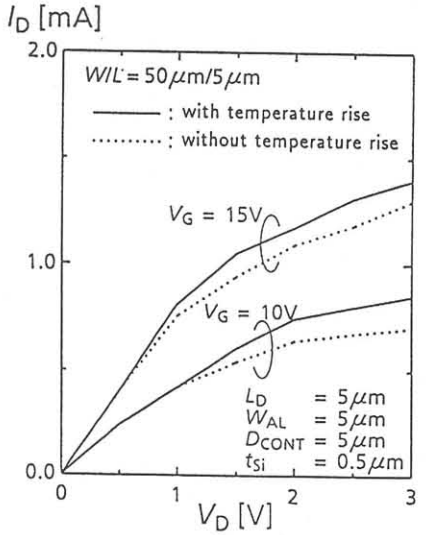


Fig.7 I_D-V_D characteristics.

the shorter channel device. These holes lower the potential barrier between the source and the poly-Si substrate and induce the short channel effect. In such short channel TFT device, the temperature rise becomes significant as shown in Fig.6. The temperature rise becomes more significant with increasing the drain voltage and the gate voltage since the power dissipation increases. The I_D-V_D characteristics calculated taking into account the temperature rise are shown in Fig.7 where the characteristics without the temperature rise are also shown for the comparison. As is clear in the figure, the drain current is increased by taking into account the temperature rise. This means that the potential barrier height at the grain boundary is lowered when the temperature rises. The temperature rise is significantly dependent on the substrate material, the poly-Si film thickness and the design rule as shown in Figs.8, 9 and 10. The temperature rise is drastically decreased if the oxidized Si wafer is used as the substrate. The thinner poly-Si film thickness gives rise to the larger temperature rise. As for the influences of the design rule, the temperature rise is significantly suppressed by increasing the Al wiring width.

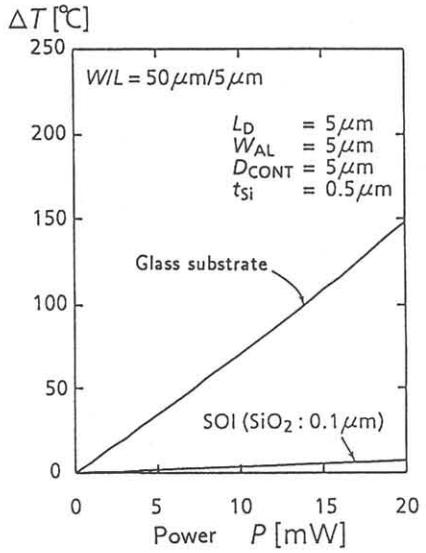


Fig.8 Temperature rise vs. power consumption changing the substrate material.

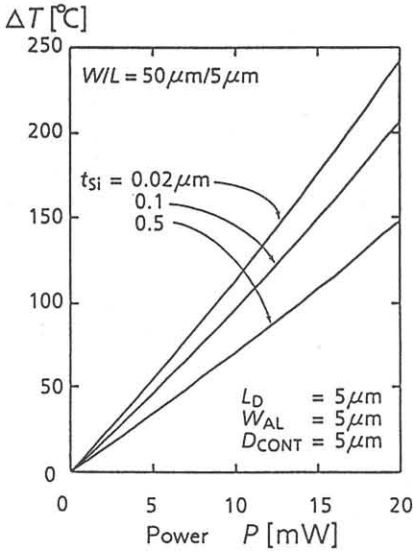
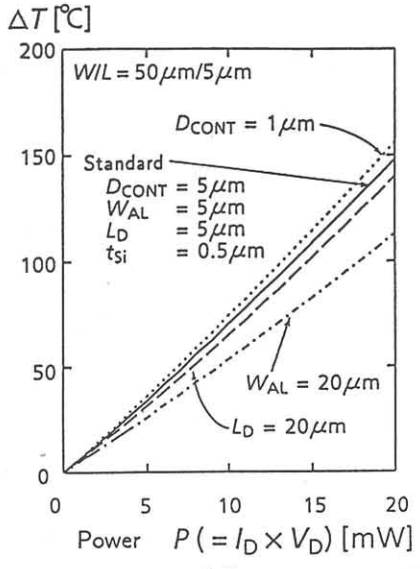
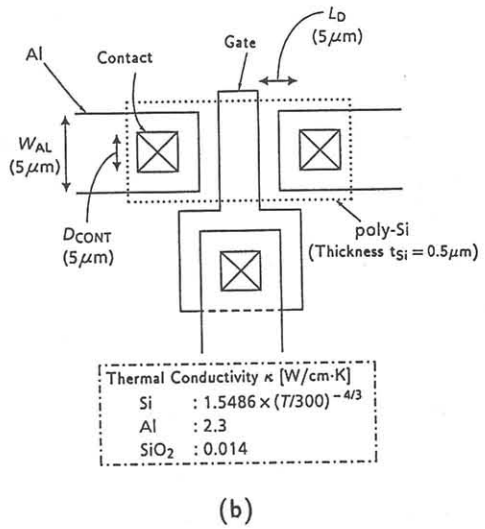


Fig.9 Temperature rise vs. power consumption changing the poly-Si thickness.



(a)



(b)

Fig.10 Temperature rise vs. power consumption changing the design rule.

4. Conclusion

We developed a new poly-Si TFT device simulator with quasi three-dimensional temperature analysis. The temperature rise effect and the avalanche short channel effect in the short channel poly-Si TFT were accurately analysed using this simulator.

References

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