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Simulation of Tunneling Current due to Enhanced Electric Fields at the Edge of Gate Electrode

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Tunneling current enhancement due to electric field concentration at a gate edge is investigated by numerical calculation. The detailed current distribution and change of current-voltage(I-V) characteristics are calculated for several gate geometries different in curvature radius. It is shown that the current density at the gate edge varies by 3 orders of magnitude with the curvature radius from 30nm to 2nm. A very narrow region of 8nm at the curvature area is responsible for 80% of the total current between the gate and n^+ region. A calculated change in I-V characteristics is found also in experimentally measured I-V curve of a poly-Si gate/SiO2/n^+-Si structure.

1.INTRODUCTION

For the operation of programming and erasing of flash memory devices, high field electron injection is utilized to remove electrons from the floating gate electrode. The electron injection is done at an edge of the floating gate such as shown in Fig.1, where the electric field concentration occurs and the tunneling current is affected by the enhanced fields.[1] Since tunneling current strongly depends on electric field, a subtle change of edge geometry can cause a significant increase or decrease of the current. To achieve stable programing and erasing characteristics, properties of the current enhancement at such a curved region need to be well characterized.

In this presentation, we evaluate the tunneling current at the curved region of the gate edge by numerical calculation. The curvature radius of polysilicon gate edge tends to be relatively large (~10nm) since it is subjected to high temperature of about 900 °C during the subsequent processing. Therefore, calculation was done for MOS structures with this range of curvature radius and thin gate oxide thickness (12nm). The detailed distribution of injection current and effects of curvature radius are examined. We demonstrate that a very narrow region less than 8nm should be properly designed to control the tunneling current.

2.METHOD FOR CALCULATING TUNNELING CURRENT

Assuming the free electron gas model in metal and the WKB approximation for the tunneling process of electron from the metal into the oxide, tunneling current density (**Jt**) and tunneling probability(**Dt**) is expressed by the following equations.[2]

$$Jt = \frac{4\pi qm_0 kT}{h^3} \int_0^\infty D_t(E_n)\ln\{1+\exp[(E_F-E_n)/kT]\}dE_n \quad (1)$$

$$D_t = \exp\left\{-\frac{4\pi}{h}\int_{l1}^{l2}[2m_{ox}(\psi_t(l)-E_n)]^{1/2}dl\right\} \quad (2)$$

The symbols represent their usual physical meanings. En is the normal component of the energy of incident electron to the metal/SiO2 interface.

The tunneling barrier profile ψ_t is expressed using the potential profile $V(l)$ near the injecting electrode surface as

$$\psi_t(l)=\phi_B-\{V_0-V(l)\} \quad (3)$$

where ϕ_B is the barrier hight at the gate/SiO2 interface and **Vo** is the potential of the injecting electrode.

The well known Fowler-Nordheim relation[3] described below is an approximated analytical expression on the assumption that the electric field is uniform toward the normal direction to the metal surface.

$$J_t=\frac{q^3 m_0}{8\pi h m_{ox}\phi_B}e^{-\frac{8\pi(2m_{ox})^{1/2}\phi_B^{3/2}}{3qhF}} \quad (4)$$

The total tunneling current is obtained by integrating the current density over the emitting electrode surface.

The calculation method we used is the same as the reference[1] except the following two points: (1) tunneling barrier was calculated along electric flux line;(2) potential was calculated numerically by the field analysis program[4] instead of Schwartz-Christoffel

transformation.[1]

The edge structure used for the calculation is shown in Fig.1. A gate electrode with a rounded corner faces toward the substrate with the distance of 12nm. The corner is shaped by an arc with a right center angle. The electron effective mass (m_{ox}) and the barrier step at the gate/SiO2 interface(ϕ_B) was set to m_o/2 and 3 eV respectively.

3.RESULTS OF THE TUNNELING CURRENT CALCULATION

Fig.2 shows the profile of tunneling current density along the gate electrode surface for different curvature radii. The profiles have a peak at the curved region. The maximum current changes from 0.01 to 10 A/cm2 depending on the curvature radius from 30nm to 2nm. The maximum current strongly depends on the curvature radius. The current decays toward the parallel plate region to a value corresponding to its nominal field (applied voltage/oxide thickness). The decay length is approximately 10nm as expected from the oxide thickness of 12nm. It should be noted that the maximum current density is very large compared to that at the parallel plate region.

The ejection of electron from the floating gate during erasing operation of a flash memory is done between floating gate and n^+ source region. To know the effect of the curvature radius to erasing characteristics, change of the total current due to the edge geometry should be evaluated. The hatched area in Fig.3 shows the region where 80% of the total current flows. The total overlap width of n^+ region and the gate was assumed to be 50nm. This figure indicates that 80 % of the total current between the gate and n^+ source region is dominated by the current flowing the very narrow region at the curved surface whose width is less than 8nm. Thus the dominant factor which determines the magnitude of the total tunneling current is not the width of overlap but the geometrical shape of the gate surface at the curved region.

In Fig.4 the calculated I-V characteristics is shown to see the effect of current enhancement to I-V curve. The solid curve incorporates the current enhancement at the edge and the dotted curve does not. At lower fields, the deviation of the two curves gets more distinctive.

This is explained by the field dependence of the current enhancement factor at the edge. The ratio of the field at the edge to the field at the parallel plate region remains constant with changing nominal field. However, the current enhancement factor, the ratio of the current at the edge to the current at the parallel plate region, will depend on the nominal field strength since the tunneling current is an exponential function of electric field. Fig.5 shows the dependence of the current enhancement factor on the nominal field. As the nominal field is decreased, the current enhancement factor increases indicating the larger contribution of the edge current to the total current at low fields.

4.COMPARISON WITH EXPERIMENTAL RESULTS

To observe the enhancement of tunneling current experimentally, we measured I-V curves of two MOS structures which are different in perimeter length of the gate electrode but have the same gate oxide area of 8.1×10^{-3} cm^2. Sample A is a MOS transistor with a 1um gate length and extremely wide gate width of 0.8m to make easy to observe edge current. Sample B is a MOS capacitor isolated by LOCOS whose total perimeter was 3.6cm. Since the total gate perimeter of the sample A is far longer than the sample B, the edge effect is expected to be observed for the sample A.

Fig.6 shows the measured I-V curves of the two samples. The difference of the current is mainly due to the work function difference between the two structures. To discern the effect of tunneling current enhancement, we should pay attention to the slight difference in the slopes of the two curves. A parallel curve to the curve B is shown in Fig.6 to focus the difference of the slope. The slope of the sample A, which have an extremely long gate edge width, is smaller than the other. This tendency is in accordance with the calculated I-V curves shown in Fig.4

5.SUMMARY

Tunneling current enhancement due to electric field concentration at a gate edge was investigated by numerical calculation. The maximum current is several to several thousands times larger than the value at the parallel plate region depending on the curvature radius. If the gate-source overlap region of 50nm is assumed, 80% of the total current flows at the curvature region whose width is less than 8nm.

To find the detailed profile of the tunneling current experimentally and fit to the calculated results may be quite difficult. However, we believe that this kind of calculation presented here provides a method to estimate the effect of surface geometry to the tunneling current and helps to devise gate edge structures and fabrication processes optimized for flash memory operation.

REFERENCE
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[3] M. Lenzlinger and E. H. Snow, J.Appl. Phys.40(1969)278.
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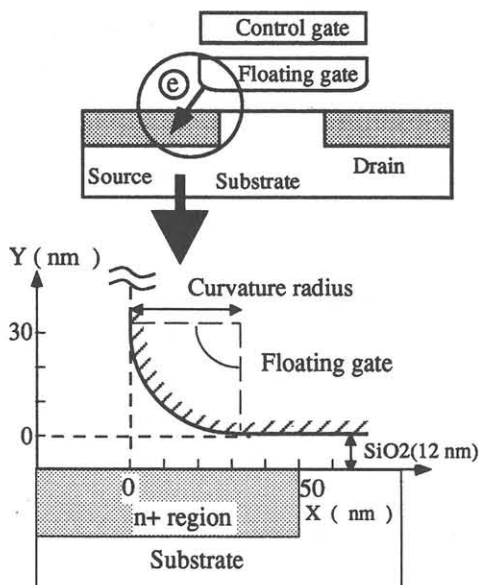
Fig.1 Cross section of a flash memory cell and the coordinate system for the tunnel current calculation.
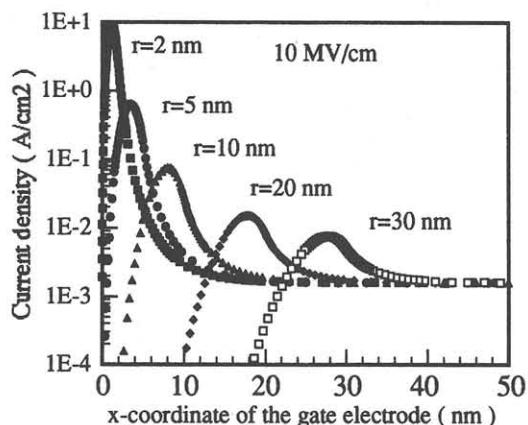

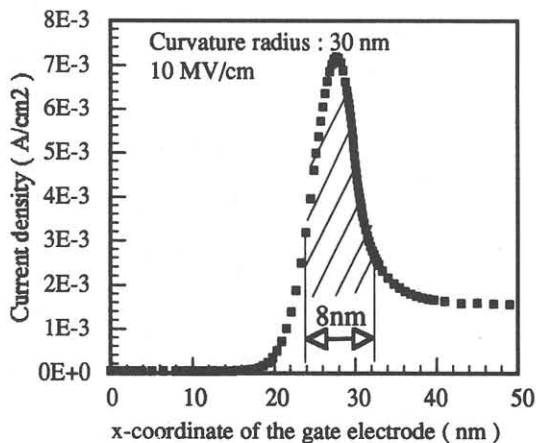Fig.2 Profile of tunneling current along the gate electrode surface for different curvature radii.

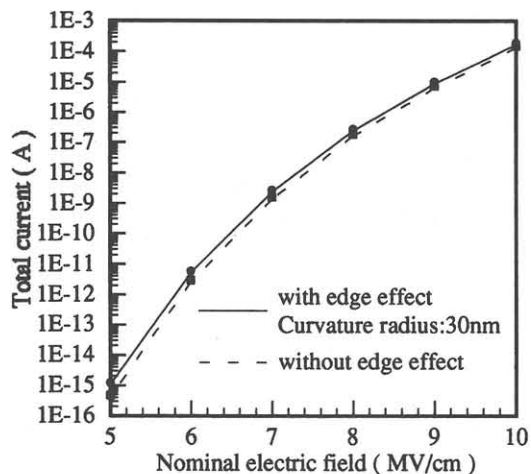Fig.3 The region where 80% of the total current flows(the hatched area).

Fig.4 Caluculated current-field curves for two cases: with edge effect and without edge effect.
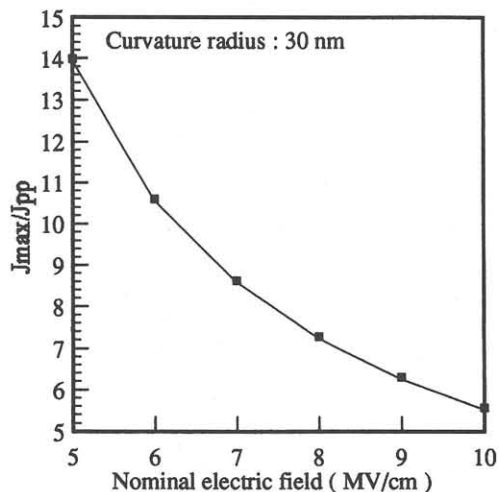

Fig.5 Current enhancement factor (J_{max}/J_{pp}). J_{max} is the maximum current density and J_{pp} is the current density at the parallel plate region.
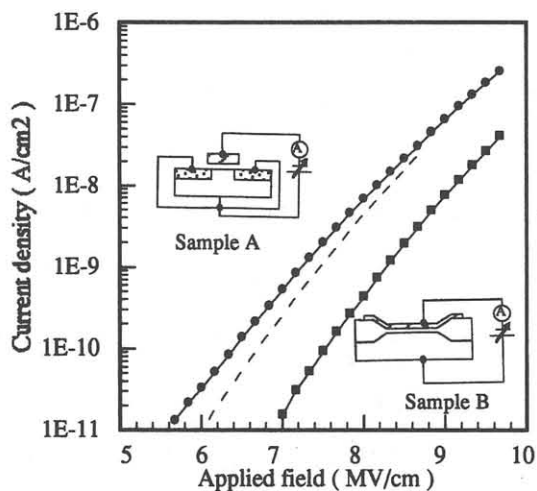

Fig.6 Measured current-field curves for MOS structures with a long gate edge perimeter (Sample A) and without(Sample B). The dashed line is parallel line to the curve B.