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Stress-Induced Quasi-Hetero-Emitter Band Structure for a Phosphorus-Doped Poly-Si Emitter Bipolar Transistor

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A novel band discontinuity is observed at the interface between a poly-Si layer, which is crystallized from an in-situ phosphorus doped amorphous Si film, and a Si substrate. The discontinuity is caused by residual tensile stress in the poly-Si layer, and forms a potential barrier for electrons and holes. The band discontinuity is proved to be the origin of HBT (Hetero-junction Bipolar Transistor)-like characteristics which were reported recently for a bipolar transistor using this poly-Si layer for the emitter.

1. Introduction

In-situ phosphorus doped poly-Si layers have been proposed for emitter materials of future Si bipolar transistors[1]. Recently, we and our co-workers reported a bipolar transistor having a poly-Si emitter which was crystallized from an in-situ phosphorus-doped amorphous Si layer[2],[3]. The transistor demonstrated HBT (Hetero-junction Bipolar Transistor)-like characteristics, that is, over ten times higher current gain than that of conventional poly-Si emitter transistors and a further increase at lower temperatures. Such very high emitter efficiency is expected to be necessary for future high-speed bipolar transistors in order to prevent the reduction in current gain due to a highly doped base. We thought that the HBT-like characteristics were due to a potential barrier for holes at the interface between the poly-Si emitter and the Si substrate. However, the origin of the barrier has not been clear until now. In this paper, we report on our investigation about structure of the barrier, that is, band structure at the interface, and its relation with residual stress and crystallographic structure in the emitter.

2. Experimental and Analytical Methods

The band structure at the interface was investigated using electrical properties of the poly-Si emitter transistors and I-V characteristics of the interface. The structure and the fabrication process of the bipolar transistors was basically the same as those in Ref. (1). I-V characteristics of the interface were measured using Kelvin patterns, the cross section of which is shown in Fig. 1. These made it possible to measure I-V characteristics only at the interface excluding contributions from other parts. Poly-Si layers with thickness of 100 to 150 nm were crystallized from phosphorus doped amorphous films, which were deposited on a (100) substrate by conventional LPCVD at 520°C using a mixture of PH_3 and Si_2H_6 for the source gas. The annealing temperature for the crystallization was 700 to 760°C. The phosphorus concentration in the layer was 3×10^{19} to 4×10^{20} cm^{-3}.

It is known that the band structure of Si varies due to lattice deformation with stress and the variation depends on the crystallographic orientation of the stress[4]. To investigate the relation between the potential barrier and stress at the interface, lattice deformation and crystallographic orientation of the grains in the poly-Si layers were measured by X-ray diffraction. The band structure derived from the electrical measurements was compared with that calculated by deformation potential theory[5],[6] using the measured lattice deformation.

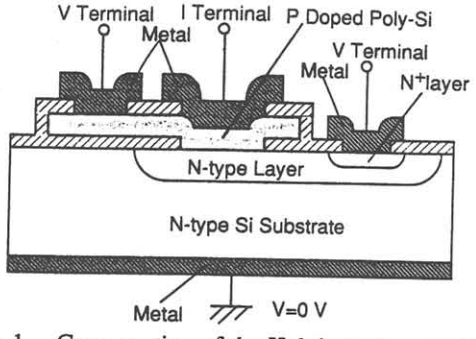

Fig. 1 Cross section of the Kelvin pattern used for measurement of interface I-V characteristics.

3. Results and Discussion

3-1. Electrical Measurements

Unique characteristics were found for our poly-Si emitter transistors, that is, correlation of the emitter efficiency with the emitter resistance (R_E) and their dependence on temperature . As shown in Fig. 2, current gain (hFE), which is proportional to emitter efficiency, is higher for the transistors with lower R_E. These plots are for transistors on the same sample. This correlation is

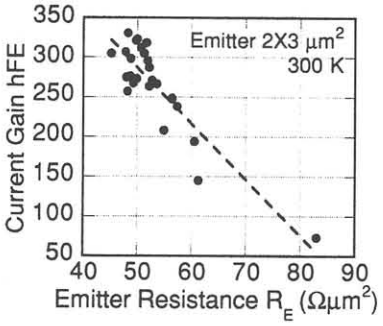

Fig. 2 Relation between current gain hFE and emitter resistance R_E for the poly-Si emitter transistors.

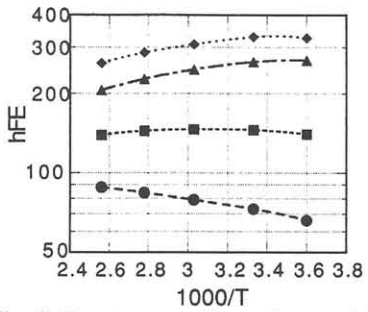

Fig. 3 Temperature dependence of the current gain hFE for the transistors of different hFE.

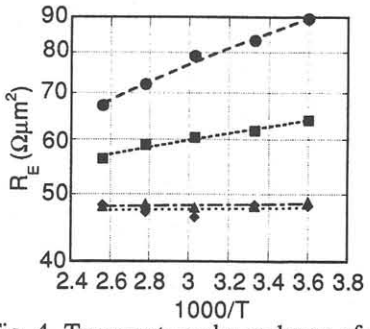

Fig. 4 Temperature dependence of the emitter resistance R_E for the transistors of different R_E.

the reverse of the case in which hFE is high due to a thin oxide layer at the poly-Si interface with a substrate[7].

Figure 3 shows temperature dependence of hFE for several transistors of different hFE values. The hFE increases at lower temperatures for the high hFE transistors but decreases for the low hFE transistors. Figure 4 shows temperature dependence of R_E for the same transistors as in Fig. 3. R_E increases at lower temperatures for high R_E transistors but is constant for low R_E transistors. From these characteristics, the band structure of the emitter is assumed to be like Fig. 5. That is, there is a potential barrier for electrons on the conduction band and for holes on the valence band at the interface, and their height dominates R_E and hFE values respectively. The solid lines are for the transistor with high R_E and low hFE, and the dashed lines are for the transistor with low R_E and high hFE. The height of the two barriers is believed to vary complementarily by the same amount as the interface state density varies.

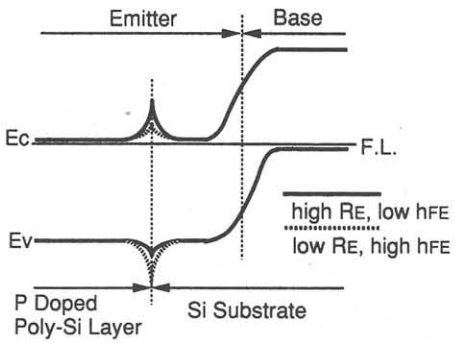

Fig. 5 The band structure of the emitter assumed from the transistor characteristics.

The measurement of the interface I-V characteristic made it possible to estimate the fine structure of the potential barriers. Figure 6 shows the results for a Kelvin pattern whose phosphorus concentration in the poly-Si layer is equal to that in the substrate. The interface indicated a rectification action like a Schottky diode. Other phosphorus concentration profiles also showed rectification action in the same direction. However, the I-V characteristic was completely linear for a conventional phosphorus implanted poly-Si layer with the same annealing temperature. Therefore, the rectification action is not due to an interfacial oxide layer, but to band transformation at the interface.

Putting these results together, the band structure at the interface was assumed to be like Fig. 7. That is, there is a potential barrier for electrons in the conduction band and for holes in the valence band due to the band discontinuity at the interface. The discontinuity of the conduction band was estimated to be about 0.1 to 0.3 eV from the forward I-V characteristics by the same method as for estimation of Schottky barrier height.

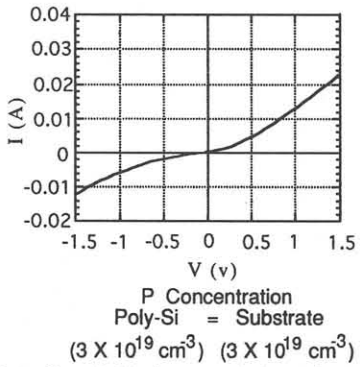

Fig. 6 Interface I-V characteristics when phosphorus concentration in the ploy-Si layer is equal to that in the substrate.

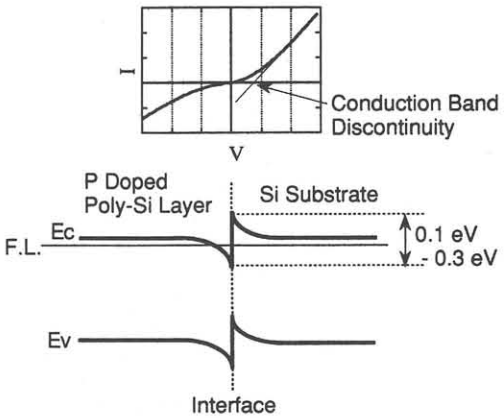

Fig. 7 Band structure estimated from I-V measurement.

3-2. X-ray Diffraction

The preferential crystallographic orientation in the poly-Si layer was estimated from the relative intensity of peaks in the X-ray diffraction pattern. The (111) peak was over a hundred times larger than the other peaks. This result indicates that almost all the grains in the poly-Si layer are oriented in the (111) direction as in Ref. (8).

The lattice deformation was measured using the shift of the (111) peak. The deformation in the direction

perpendicular to the surface $\Delta a_\perp/a_\perp$, which was derived directly from the peak shift, was -2.6×10^{-3}. Here, $a_\perp$ is a lattice constant perpendicular to the surface and $\Delta a_\perp$ is its variation. For the direction parallel to the surface, the deformation $\Delta a_{II}/a_{II}$ was evaluated using Poisson's ratio of a (111) oriented Si film[4], which relates the parallel deformation to the perpendicular one under uniform biaxial stress. The result was $+6.0 \times 10^{-3}$. In this calculation, reduction of lattice constants due to incorporation of phosphorus atoms was neglected. This reduction was estimated to be about 1×10^{-4} for the poly-Si layer employed in this measurement. The results mentioned above are shown schematically in Fig. 8, which indicates that the poly-Si layer has tensile stress of about 1 GPa. On the other hand, compressive stress is believed to operate on the substrate surface as a reaction to the tensile stress in the poly-Si layer.

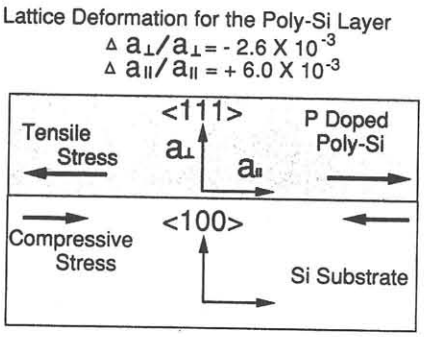

Fig. 8 Lattice deformation and crystallographic orientation at the interface measured by X-ray diffraction.

3-3. Variation of Band Structure due to Stress

Variation of the band structure due to the lattice deformation was calculated by deformation potential theory[5], [6]. According to the theory, the symmetry breaking component of the deformation splits the degenerate band edges, and the hydrostatic component shifts the energy without splitting. Figure 9 shows the band edge energy shift at the interface under tensile deformation in the poly-Si layer and compressive deformation in the substrate as in Fig. 8. $dE/d\ln a_{II}$ indicates the energy shift rate for variations of a_{II}. Important variations are an increase in electron affinity for the poly-Si layer and a decrease for the substrate mainly due to the hydrostatic component. These variations cause band discontinuity at the interface just as in Fig. 7.

The band structure for the case of Fig. 8 was calculated to be as shown in Fig. 10. The conduction band discontinuity was 0.096 eV assuming that the compressive stress intensity in the substrate was the same as the tensile one in the poly-Si layer at the interface. The value of 0.096 eV is small compared with the values of 0.1 to 0.3 eV from the I-V characteristics in Fig. 7. However, considering the difficulty in measuring the lattice constants exactly at the interface and the inaccuracy of the discontinuity values from the electrical measurement due to the presence of interface states, this discrepancy is tolerable. Therefore, we conclude that the band structure calculated from the stress coincides with that estimated from the electrical measurements on the whole. Another important point is that the band-gap reduction for the (111) oriented poly-Si layer is much less than for the (100) substrate. This small band-gap change under the stress is essential for the formation of the large potential barrier in the valence band.

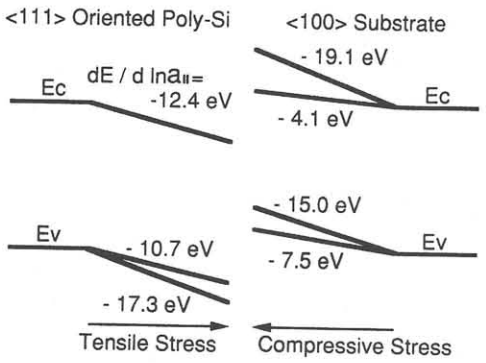

Fig. 9 Band edge energy shift due to the deformation at the interface calculated by deformation potential theory[4], [5].

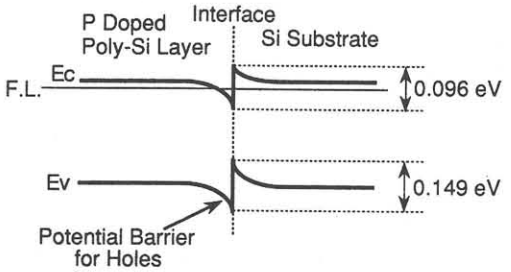

Fig. 10 Band structure calculated by deformation potential theory using measured lattice deformation.

4. Conclusion

We have clarified the cause of the HBT-like characteristics of a bipolar transistor that has a poly-Si emitter which is crystallized from an in-situ phosphorus doped amorphous Si film. The poly-Si emitter, which consists of grains of (111) crystallographic orientation, has strong tensile stress of about 1 GPa. Due to the structure and the stress, a band discontinuity is formed at the interface with the substrate. The band discontinuity induces a potential barrier for holes, which is the cause of the HBT-like characteristics.

Acknowledgments

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