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# Multi-drain/Multi-collector Structured Full-Swing Complementary BiCMOS Buffers

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**Abstract :**

Novel circuit techniques for increasing the voltage swing of complementary BiCMOS (CBiCMOS) buffers, employing multi-drain/multi-collector structures, are proposed. These circuit techniques ensure that the implemented pnp BJT's do not appreciably affect the speed performance. These circuits offer near rail-to-rail output voltage, less circuit complexity, less process complexity, and high speed performance at scaled down power supply voltages (< 2V). The new circuits have been simulated and compared to conventional BiCMOS and CBiCMOS buffers.

## I- Introduction :

The degradation in the speed performance of the conventional BiCMOS driver at reduced supply voltages prohibits fast switching, especially if the load capacitance is large [1]. Therefore, the conventional CBiCMOS, the full swing CBiCMOS and other structures have been proposed to overcome this problem [2,3]. However, the conventional CBiCMOS driver suffers from partial swing operation [2]. On the other hand, the full swing CBiCMOS buffers require high performance pnp BJT (with a consequent increase in the process complexity) and suffer from increased circuit complexity (extra devices per gate) [3].

In this work we introduce three new configurations of complementary BiCMOS buffers (CBiCMOS-A, CBiCMOS-B, and CBiCMOS-C). These complementary BiCMOS circuits (Fig. 1) have been configured in a way so that the pnp BJT's are implemented only in the internal parts of the circuits, while the npn BJT's are employed as output drivers. This allows the implementation of non-optimized pnp BJT's with little additional process complexity [4]. The multi-drain/multi-collector structure is implemented in the CBiCMOS-B and CBiCMOS-C buffers to isolate the bases of the BJT's [3,4]. This structure is necessary to reduce the BJT's turn-off time, ensure full-swing operation and improve speed performance at lower supply voltage (< 2V) with no penalty of circuit complexity. Simulation results, using SPICE, confirm these conclusions.

## II- Circuit Description and The Theory of Operation :

The CBiCMOS-A circuit is depicted in Fig. 1(a). The pull-up part of this circuit is similar to that of the conventional BiCMOS one [2]. M1 is employed to drive Q1 and to discharge the base of Q3 during the pull-up operation. Whereas M2 functions to discharge the base of Q1 and to drive Q3, while the collector current of Q3 drives Q2 during the pull-down operation.

The transient operation of the CBiCMOS-A driver for the input rising transition is explaind as follows : when the input voltage rises from "LOW" to "HIGH", M2 turns on causing Q3 and in turn Q2 to enter into the active region. The output node is hence being pulled-down and when the output voltage reaches the BJT turn-on voltage ($V_{be,on}$) Q3 turns off. It is, therefore, difficult to attain the full swing condition, especially at low supply voltage values (< 2.5 V).

Figure 1(b) shows the CBiCMOS-B circuit. In this circuit the multi-drain/multi-collector structure of M2 and Q4 (or M3 and Q3) is implemented to isolate the bases of the BJT's Q1 and Q3 (or Q2 and Q4) [3,4]. The transient operation of this circuit is explained as follows : when the input rises from "LOW" to "HIGH" the NMOS M2 turns on, causing Q3 and in turn Q2 to, eventually, enter into the saturation region. The output node is hence pulled-down to the collector-emitter saturation voltage ($V_{ce,sat}$). The pull-up process can be similarly

explained. The circuit technique, introduced here to obtain the full–voltage–swing, is based on saturating the BJT's by using a DC base current [5]. As a result, the DC power consumption and the BJT's turn–off time are increased.

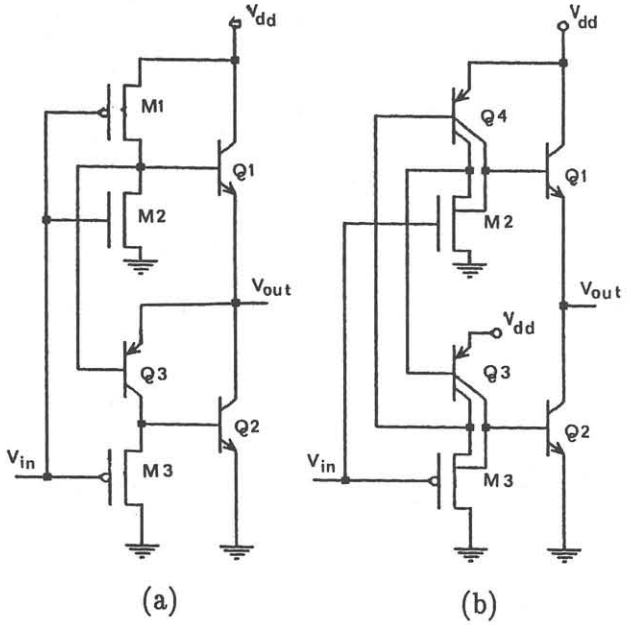


**Fig. 1** : Schematics of the (a) CBiCMOS–A, and (b) CBiCMOS–B buffers.

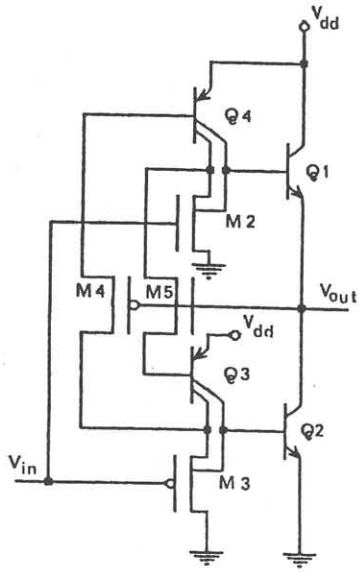


**Fig. 1** (c) : Schematic of the CBiCMOS–C buffer.

Figure 1(c), illustrates the CBiCMOS–C circuit. The principle of operation of this circuit is similar to that of the CBiCMOS–B one. However, the NMOS M5 and the PMOS M4 are employed to control the base current of Q3 and Q4, respectively. The conduction of M4 and M5 is controlled by the output voltage. In this implementation the size of M4 (or M5) can be tailored to allow the output voltage to get as close as possible to $V_{dd} - V_{ce,sat}$ (or $V_{ce,sat}$) before the base current of Q4 (or Q3) falls to zero to ensure the full–voltage–swing operation [3]. Therefore, there is no DC power consumption and the BJT's turn–off time is further reduced.

When optimizing each of the conventional BiCMOS, CBiCMOS, CBiCMOS–A, CBiCMOS–B, and CBiCMOS–C for minimum delay, the ratio of the areas is approximately equal to 0.67 : 0.67 : 0.75 : 0.83 : 1.0, respectively.

**III– Simulation Results and Discussion :**

Circuit simulation employing 0.5 $\mu$m BiCMOS technology device parameters has been performed using SPICE. The simulation cut–off frequencies for npn and pnp BJT's are 9 GHz and 3.6 GHz, respectively. The new circuits have been simulated and compared to the conventional BiCMOS and CBiCMOS circuits.

The simulated degradation in the propagation delay–time ($t_{pd}$) of the above circuits with the power supply voltage ($V_{dd}$) when the load capacitance is equal to 5 pF is shown in Fig. (2). In comparison to the conventional BiCMOS and CBiCMOS buffers, the new circuits have better delay to power supply voltage sensitivity and hence better speed performance. The CBiCMOS–B and CBiCMOS–C operate efficiently even for power supply voltages lower than 2 V while, the CBiCMOS–A operates efficiently only at supply voltages greater than 2.5 V.

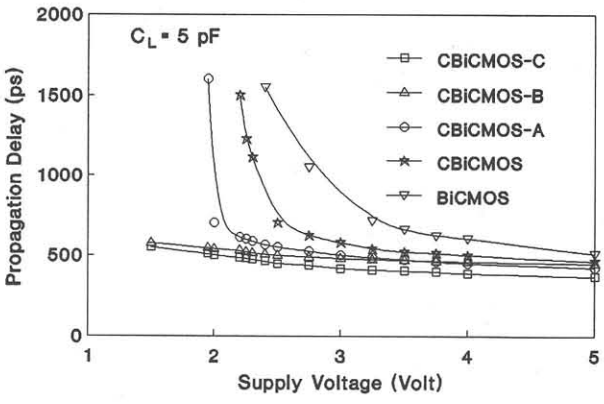


**Fig. 2** : The simulated delays of the five circuits versus supply voltage with $C_L$ = 5PF.

Figure 3 shows the dependence of the propagation delay–time of the above circuits on the load capacitance $C_L$ when the supply voltage is equal to 2.5 V. The new CBiCMOS buffers show better speed performance and

better delay to load sensitivity compared to the conventional BiCMOS and CBiCMOS buffers. The delay to load sensitivity S (ps/pF) of the conventional BiCMOS, CBiCMOS, CBiCMOS–A, CBiCMOS–B and CBiCMOS–C is equal to 232, 116.3, 81, 75, and 65 ps/pF, respectively, when the supply voltage is equal to 2.5 V.

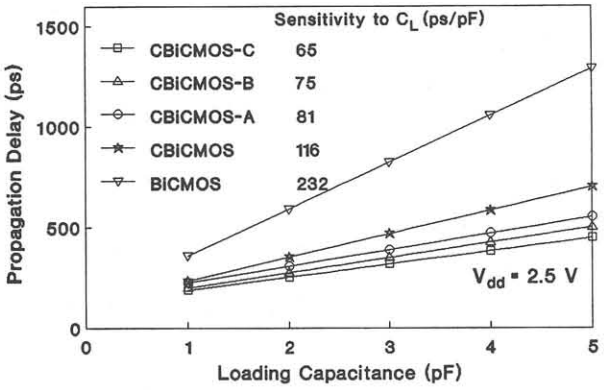


**Fig. 3** : The simulated delays of the five circuits versus load capacitance for Vdd = 2.5V.

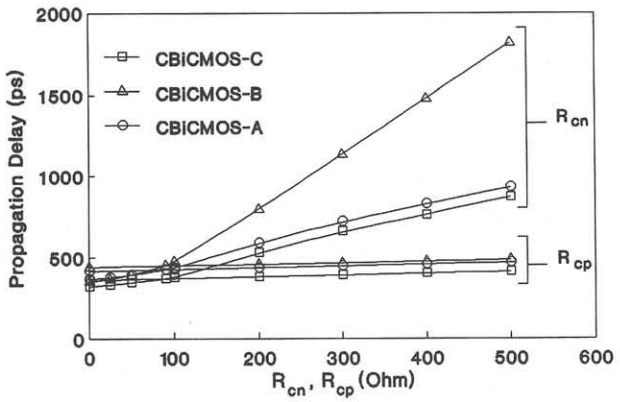


**Fig. 4** : Effect of the collector resistances, Rcn of Q2 and Rcp of Q3 on the simulated delays of the three proposed CBiCMOS buffers.

Figure 4 shows the delay–time (tpd) of the new CBiCMOS buffers as a function of the the collector resistance Rcn and the collector resistance Rcp of the npn BJT Q2 and the pnp BJT Q3, respectively, for 5 V supply voltage with a load capacitance equal to 5 pF. It is indicated that the effect of the collector resistance Rcp of the pnp BJT Q3 is negligibly small compared to the effect of the collector resistance Rcn of the npn BJT Q2 on the propagation delay. Consequently, the new circuits allow the implementation of non–optimized pnp BJT's with little additional process complexity [4].

In comparison to the full swing complementary BiCMOS buffer [3], the CBiCMOS–C buffer has less circuit complexity (8 instead of 14 discrete devices), less area (approximately 30% area saving), less process complexity (implementation of non–optimized pnp BJT's), symmetrical pull–up and pull–down structures, and is efficient even for supply voltages lower than 2 V.

## IV– Conclusion :

Three configurations of CBiCMOS (CBiCMOS–A, CBiCMOS–B and CBiCMOS–C) buffers have been proposed. These new circuits have better delay to supply voltage sensitivity, better delay to load sensitivity and high speed performance, compared to the conventional BiCMOS and CBiCMOS circuits, at scaled–down supply voltages. Among the three introduced circuits the CBiCMOS–A has the smallest area and comparable speed performance for 2.5 V supply voltages but suffers from partial swing operation. On the contrary, the CBiCMOS–B and CBiCMOS–C buffers show high speed and full swing operation at reduced supply voltages (< 2 V). Furthermore, the CBiCMOS–C buffer has no DC power consumption, compared to the CBiCMOS–B one.

Employing the pnp BJT's only in the internal parts of the complementary BiCMOS circuits allows the implementation of non–optimized pnp BJT's (less process complexity). In BiCMOS, the implementation of the proposed multi–drain/multi–collector BiCMOS structure is efficient to isolate the bases of the implemented BJT's and to reduce the BJT's turn–off time for better speed performance. Moreover, this structure offers less circuit complexity (reduce the number of devices per gate) and area saving.

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