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A Poly-Si TFT Process for High Speed and Low Voltage CMOS Circuits

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A poly-Si TFT process for high speed and low voltage CMOS circuits which is applicable to HDTV LCDs with integrated drivers has been developed. The defects in the poly-Si film are extremely reduced by the annealing in O_2 ambient (O_2 annealing) after the solid phase crystallization of LPCVD α-Si. The field effect mobilities of NMOS and PMOS TFTs are 140cm²/Vs and 110cm²/Vs, respectively. The CMOS shift registers operate at frequencies as high as 35MHz under a supply voltage of 14V. By reducing the gate length, the maximum frequency of 9.5MHz is achieved under a supply voltage as low as 5V.

1.Introduction

In recent years, there has been a strong demand for practical HDTV LCD systems[1][2]. The high temperature poly-Si TFT process is one of the promising candidates for very small and high resolution LCDs with fully integrated drivers, especially for HDTV projector because of the availability of VLSI technology and the simplicity of the poly-Si film formation compared with that of the low temperature process. However, more superior characteristics of poly-Si TFTs for HDTV systems than for those of conventional electronic viewfinders are yet required. Namely the grain size of poly-Si film should not only be enlarged, which is usually done by solid phase crystallization (SPC) of α-Si film, but also the defect density in poly-Si film should be reduced.

In this work, we have successfully developed a poly-Si TFT CMOS process applicable to HDTV-class LCDs with fully integrated drivers. The effects of O_2 annealing on the reduction of defects in the poly-Si film after SPC are examined by the characterization of poly-Si crystallinities and the evaluation of device performance. Further the CMOS shift registers are fabricated by this process including O_2 annealing to evaluate the applicability to high speed and low voltage CMOS circuits.

2.Experiments

High quality poly-Si film formation consists of two steps, i.e., SPC in order to enlarge the grain size and following O_2 annealing to decrease the defects, which is schematically illustrated in Fig.1. The starting material is an 110nm thick α-Si film deposited on a quartz substrate by LPCVD (low-pressure chemical vapor deposition) using Si_2H_6 as a source gas at 450℃. In the first step, an α-Si film is crystallized at 600℃ for 24 hours in N_2 ambient (SPC). Subsequently, the poly-Si film is annealed at 1050℃ in O_2 ambient (O_2 annealing). After O_2 annealing, oxide on the surface of poly-Si is removed and then the device regions are patterned. A 85nm thick high temperature CVD oxide (HTO) is deposited at 850℃ as a gate dielectric film. After gate electrodes are patterned, phosphorus and boron ions are implanted into the source and drain regions of NMOS and PMOS TFTs, respectively, which are self-aligned to the gate electrodes. Final passivation of all devices is performed by hydrogen diffusion from PECVD SiN to terminate the dangling bonds during a subsequent annealing at 420℃ after Al metallization. By using this process, which is optimized by the following analyses, the CMOS shift registers are fabricated to prove the circuit performance.

Poly-Si films are characterized as follows. O_2 annealing time is varied from 12min. to 120min., when oxide thickness is from 35nm to 130nm., to investigate the effects on the reduction of defects in the poly-Si film. A poly-Si film is also annealed in N_2 ambient (N_2 annealing) at 1050℃ for 30min. after SPC to compare with the effects of O_2 annealing. The structures of poly-Si films are observed by transmission electron microscope (TEM) to evaluate the grain size and the defects. Electron spin resonance (ESR) is used to determine the defect density originated

from dangling bonds in poly-Si films. The surface roughness of poly-Si films is measured by atomic force microscope (AFM) after O_2 annealing.

3.Results and Discussion

Fig.2 shows TEM photographs of poly-Si films after SPC, O_2 and N_2 annealing, respectively. The grain size of poly-Si film after SPC is well enlarged and its maximum size is a few microns shown in Fig.2(a). There is no change of the grain size, but the fine structures in the grains and at the grain boundaries disappear specially after O_2 annealing for 37min. compared with N_2 annealing for 30min. at 1050℃ shown in Fig.(b) and (c), respectively. It means that the defects after O_2 annealing are less than that after N_2 annealing.

Fig.3 shows the spin density of poly-Si film obtained from ESR as a function of annealing time. The spin density decreases from $1\times10^{19}cm^{-3}$ to $5\times10^{17}cm^{-3}$ after SPC and dramatically decreases to less than $1\times10^{17}cm^{-3}$ after O_2 annealing. It reaches to $8\times10^{16}cm^{-3}$ of minimum density at 37min. and over that it slightly increases with the increase of O_2 annealing time. The spin density after N_2 annealing at 1050℃ for 30min. is $2\times10^{17}cm^{-3}$. O_2 annealing is more effective in the reduction of defects than N_2 annealing.

The mechanism of O_2 annealing is assumed as follows. During O_2 annealing, unoxidized Si interstitials formed by a small fraction of excess silicon atoms near $Si-SiO_2$ interface[3] quickly diffuse into the poly-Si film and reduce the defects existed at the grain boundaries and in the grains.

However, it is afraid that the increase of surface roughness of poly-Si films during O_2 annealing is caused by the difference of oxidation rate between the grain boundaries and each grain. The surface roughness obtained from AFM after O_2 annealing is shown as a function of annealing time in Fig.4. The surface of poly-Si film after SPC is very smooth and its roughness is a few angstroms. The surface roughness increases by O_2 annealing but it is as small as about 10Å for shorter than about 40min. For over that it gradually increases.

In summary of the analyses above mentioned, O_2 annealing is extremely effective in the reduction of defects in poly-Si films. But excessive O_2 annealing increases the surface roughness and reduces the controllability of the fabrication process with the decrease of poly-Si thickness. The optimum O_2 annealing time is around 40min. at 1050℃.

The characteristics of NMOS and PMOS TFTs fabricated by using O_2 annealing for 37min. at 1050℃, when oxide thickness is about 60nm, are measured. Fig.5 shows the drain current (ID) versus gate voltage (VG) characteristics of NMOS and PMOS TFTs with gate width of 20μm and gate lengths(Ln,Lp) of 7μm and 5μm, respectively. The field effect mobilities and threshold voltages of NMOS and PMOS TFTs are 140 cm^2/Vs, 4.0V and 110cm^2/Vs, -3.9V, respectively. High performance for both type of TFTs accomplishes high speed operation of CMOS circuits.

Fig.6 shows the field effect mobilities of NMOS and PMOS TFTs as a function of O_2 annealing time. The field effect mobilities of both type of TFTs fabricated by O_2 annealing are very large and over 100cm^2/Vs. They slightly improve with increasing O_2 annealing time. These results are explained by the reduction of the defects in poly-Si characterized by TEM and ESR analyses.

The characteristics of the CMOS shift registers fabricated by the process including O_2 annealing are measured. Fig.7 shows the maximum clock frequencies of CMOS shift registers as a function of supply voltage. The devices with O_2 annealing are much faster than those without annealing after SPC. When the supply voltage is 14V, the maximum clock frequencies in excess of 35MHz are achieved at gate lengths of Ln=7μm and Lp=5μm. Decreasing gate lengths to Ln=4μm and Lp=3μm, the maximum clock frequency of shift registers increases to 9.5MHz under a supply voltage as low as 5V.

4.Conclusion

O_2 annealing of the poly-Si film with large grain size obtained by SPC of LPCVD α-Si using Si_2H_6 as a source gas is greatly effective in the reduction of the defects. The field effect mobilities of NMOS and PMOS TFTs fabricated by using this technique are as high as 140cm^2/Vs and 110cm^2/Vs, respectively. The characteristics of the CMOS shift registers prove the capability for the high speed and low voltage CMOS circuits composed of these TFTs. This CMOS process certainly promises very small and high resolution LCDs with integrated drivers such as HDTV LCDs.

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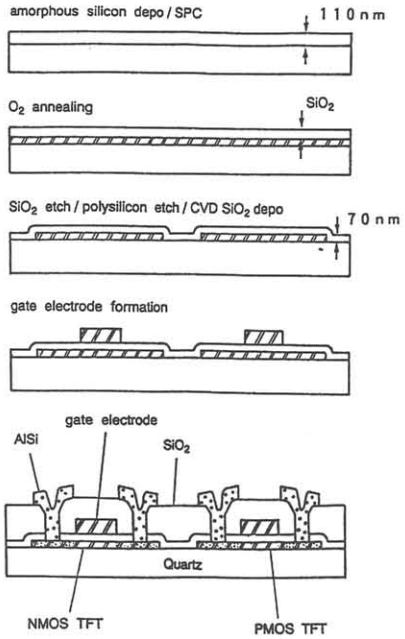

Fig.1 The fabrication process flow.

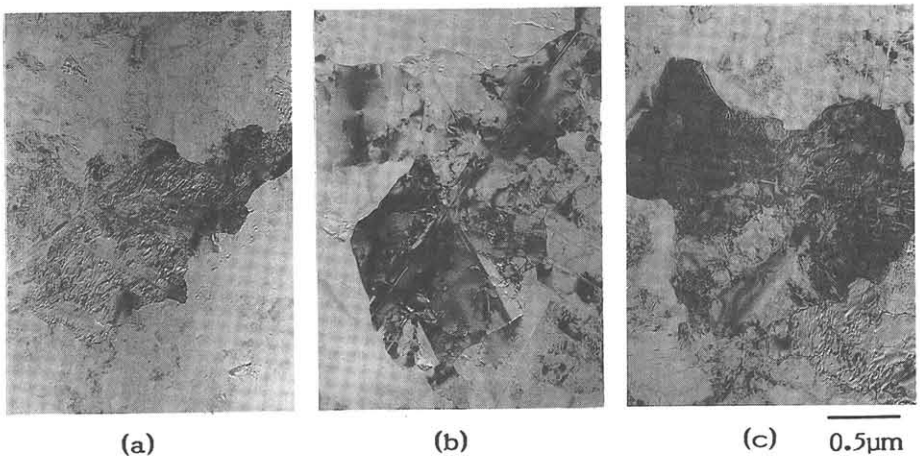

Fig.2 TEM micrographs of poly-Si film after SPC, O_2 and N_2 annealing.
(a)SPC at 600℃ for 24h.
(b)SPC at 600℃ for 24h and O_2 annealing at 1050℃ for 37min.
(c)SPC at 600℃ for 24h and N_2 annealing at 1050℃ for 30min.

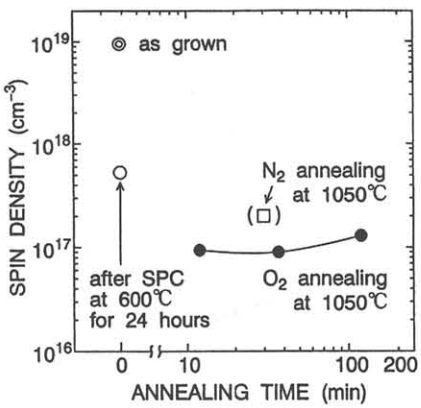

Fig.3 The spin density of poly-Si film as a function of annealing time.

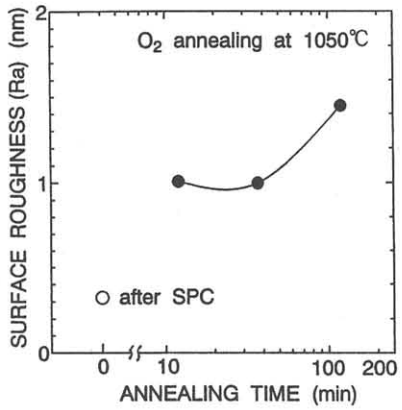

Fig.4 The surface roughness after O_2 annealig at 1050℃ as a function of annealing time.

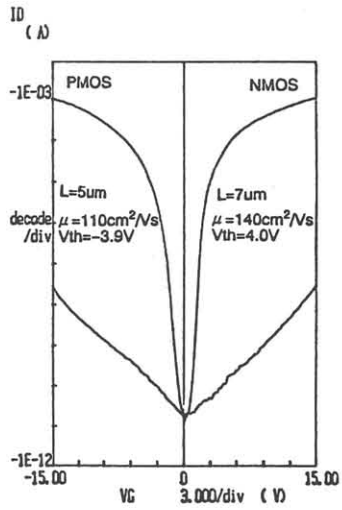

Fig.5 I_D-V_G characteristcs of NMOS and PMOS TFTs at |Vds|=10V. (W=20 μ m)

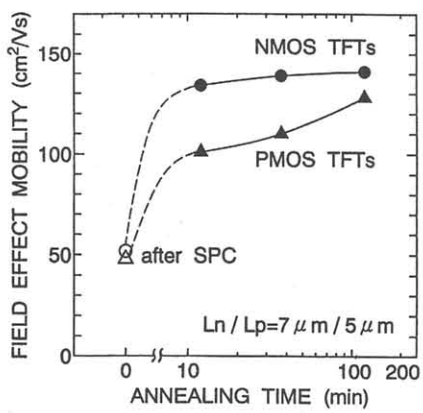

Fig.6 The field effect mobilities of NMOS and PMOS TFTs as a function of O_2 annealing time. O_2 annealing at 1050℃.

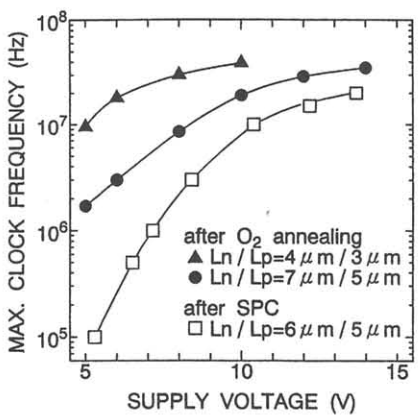

Fig.7 The maximum clock frequencies of CMOS shift registers as a function of supply voltage.