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High Performance Polysilicon Thin-Film Transistors Using Very Thin Sputtered Gate Oxide Films

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Polysilicon thin-film transistors with with various gate oxide thicknesses from 94 to 12 nm using sputter-deposited SiO_2 films were fabricated and their electrical characteristics were studied. The gate SiO_2 film was deposited by magnetron sputtering at 200℃ using a mixture of Ar and O_2 as a sputtering gas. The polysilicon TFT with a 12-nm gate SiO_2 film showed excellent characteristics: threshold voltage of 0.4 V, subthreshold slope of 140 mV/dec, field effect mobility of 77 cm^2/Vs and the gate oxide breakdown voltage of 22 V. These results indicate a possibility of improving polysilicon TFT circuit performance by scaling down the device structure.

1. INTRODUCTION

Although some studies on polysilicon thin-film transistors (TFTs) with reduced channel dimensions have been done [1-5], the full potential of achieving higher performance by reducing the gate oxide thickness has not been extensively investigated in polysilicon TFTs because of the difficulties in obtaining very thin gate oxide films keeping high quality for the gate insulator.

A sputter-deposited SiO_2 films using Ar and O_2 mixture as a sputtering gas have been developed by Suyama et al previously to achieve lower process temperature. [6-14] Superior TFT characteristics comparable or even better than those of thermally grown SiO_2 have been achieved in polysilicon TFTs using the SiO_2 films with 100 nm thickness. It has also been shown that the sputtered SiO_2 shows high dielectric breakdown strength even when the thickness is reduced to 3.5 nm. [15]

In this work, we have fabricated and characterized polysilicon TFTs with the sputter-deposited gate oxide films of various thicknesses, including 12 nm which is the thinnest, to explore the possibility of scaling down the gate oxide thickness.

2. DEVICE FABRICATION

The polysilicon TFTs were fabricated on fused quartz substrate using the following process. Original polysilicon thin films were deposited from Si_2H_6 at 470 ℃ using the LPCVD method. The polysilicon film was then thermally annealed for 15 hours at 600℃ for solid-phase crystallization [16]. It was then annealed at 800℃ for 30 min. The resulting polysilicon films have grain sizes around 1 μm. After the polysilicon island formation, SiO_2 films with thicknesses ranging from 94 to 12 nm were deposited by the magnetron sputtering method at 200℃ using an oxygen-argon mixture (30 % oxygen concentration, 5 mTorr) as a sputtering gas [6-15]. The deposition rate was 1.2 to 1.4 nm/min. The gate oxide thickness were measured on control Si wafers using elipsometry. A phosphorus-doped polysilicon film deposited by the LPCVD method was used as gate electrode. Source and drain regions were formed by phosphorus ion implantation followed by thermal activation at 800℃. The TFTs were completed after interlayer SiO_2 film deposition by magnetron sputtering, contact hole formation using reactive ion etching and metallization using consecutive DC magnetron sputtering of Mo and Al films.

3. RESULTS AND DISCUSSION

The TFT characteristics were measured and their gate oxide thickness dependency was investigated. Figure 1 shows the drain-to-source current vs. gate voltage curves of a polysilicon TFT with 12 nm gate oxide for different drain voltages. It is clearly seen that high on to off current rartio of about 10^6 is obtained at the drain-to-source voltage of 5 V.

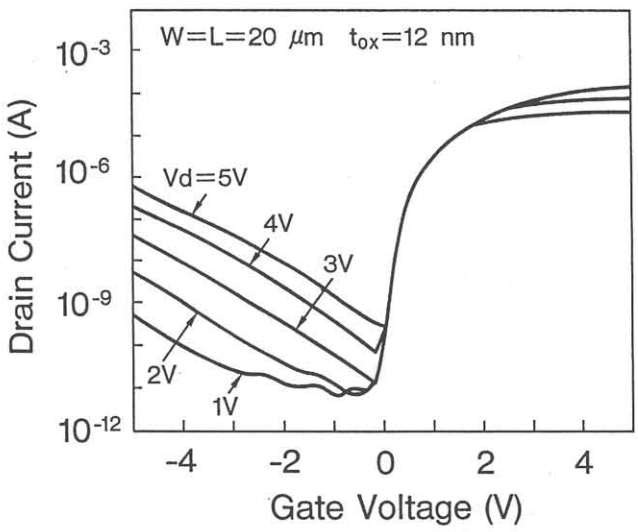

Fig. 1. Drain current vs. gate voltage curves in the polysilicon with a 12-nm- thick gate oxide.

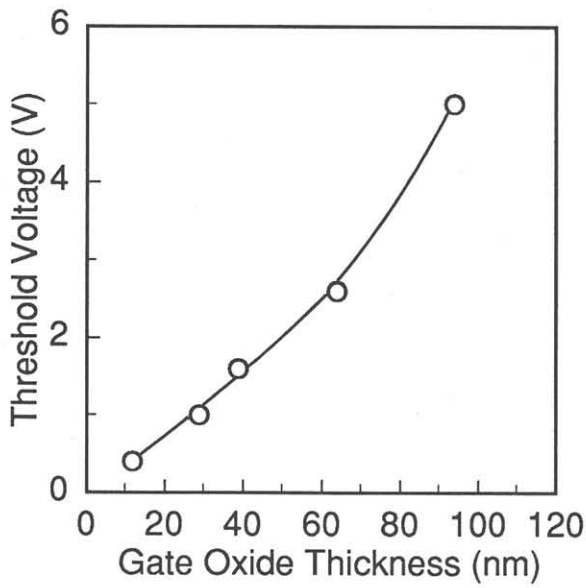

Fig. 2. Threshold voltage dependence on the gate oxide thickness.

Figure 2 shows the dependency of the threshold voltage on the gate oxide thickness. As expected, the threshold voltage shows linear decrease for smaller gate oxide thicknesses.

Figure 3 shows the relationship of subthreshold slope and gate oxide thickness. The subthreshold slope shows a remarkable steepening as the gate oxide thickness is reduced.

The subthreshold slope S can be expressed as a function of the depletion-layer capacitance C_D, the capacitance C_{it} which is associated with the trap-density, and the gate oxide capacitance C_i as follows, [17)]

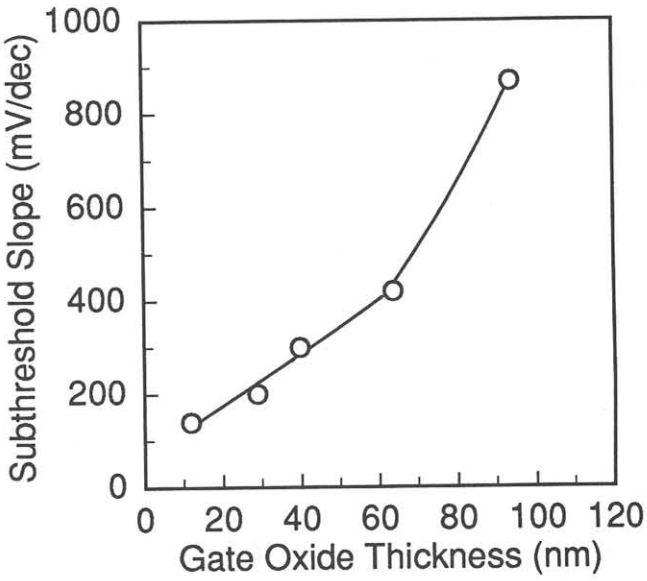

Fig. 3. Subthreshold slope dependence on gate oxide thickness.

$$S=(kT \cdot \ln 10/q) \cdot [1+(C_D+C_{it})/C_i] \qquad (1)$$

where k is the Boltzman constant, T is the temperature and q is the electron charge. The subthreshold slope decreases linearly as the gate oxide thickness is reduced from 64 nm to 12 nm. This indicates that the trap density is constant at least in the above gate oxide thickness range.

Breakdown voltage is a crucial factor that determines the applicable supply voltages. As shown in Fig. 4, it decreases with the gate oxide thickness.

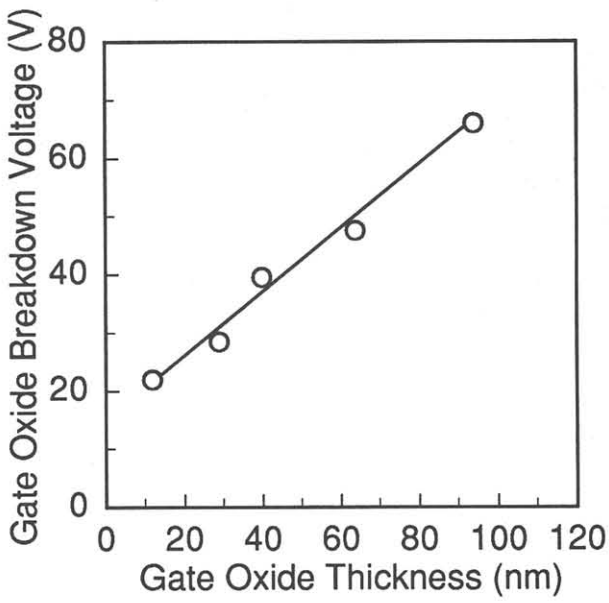

Fig. 4. Gate oxide breakdown voltage dependence on gate oxide thickness.

However, the relation of the breakdown voltage with the thickness is sub-linear indicating higher tolerance to electric field values in small gate oxide thicknesses.

The electrical characteristics of the TFT with 12 nm gate oxide is summarized in Table 1. Excellent characteristics such as threshold voltage of 0.4 V, subthreshold slope of 140 mV/dec and field effect mobility of 77 cm^2/Vs are achieved. These threshold and subthreshold characteristics are much favorable for scaled down TFTs which are supposed to be used with lower supply voltages. The breakdown voltage of 22 V allows implementation of TFT integrated circuits using a 5 V supply voltage with enough margin.

TABLE I. Characteristics of the polysilicon TFT with a 12 nm thick gate oxide.

Threshold Voltage	0.4 V
Subthreshold Slope	140 mV/dec
Field Effect Mobility	77 cm^2/Vs
On/Off Ratio (Vd=5 V)	10^6
Gate-Oxide Breakdown Voltage	22 V

4. CONCLUSION

We have demonstrated that high performance polysilicon TFTs are possible with very thin sputter-deposited SiO_2 films. We believe that this is the first report on a polysilicon TFT with deposited gate oxide film as thin as 12 nm. The results obtained in this work for thin oxide TFTs are very encouraging for circuit applications. With scaled down design, we can expect TFT integrated circuits with sophisticated processing functionality comparable with silicon VLSIs. Combining this functionality and polysilicon TFTs' unique feature that they can be built on insulating and optically transparent substrates, we believe that new applications such as parallel optoelectronic switching and processing systems will become possible in which analog and/or digital processing is done in high performance polysilicon TFT circuits. [18)]

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