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# Thin-Film Transistor Characteristics Fabricated on Nucleation-Controlled Poly-Si Films by Surface Steps

Tanemasa Asano, Kenji Makihira and Hiroomi Tsutae

*Center for Microelectronic Systems, Kyushu Institute of Technology*
*680-4 Kawazu, Iizuka, Fukuoka 820*

Polycrystalline Si films were prepared on $SiO_2$/Si substrates by solid phase crystallization of vacuum-evaporated amorphous Si with a nucleation controlled process by steps formed at the substrate surface. Crystallinity of the Si films and characteristics of n- and p-channel thin film transistors fabricated on the Si films have been investigated. The Si films were found to be composed of stripe-shaped grains elongated in the direction perpendicular to the step. The vast majority of the grains had ⟨111⟩ axis in the direction perpendicular to the substrate surface. Concerning the crystal orientation in-plane, a tendency that ⟨211⟩ axis aligns to the direction perpendicular to the step was found. Both n- and p-channel transistors fabricated on the Si films showed improved channel carrier mobility and subthreshold slope compared with those fabricated on Si films prepared by solid phase crystallization without nucleation control. The improvement was more pronounced in n-channel transistors, which suggested that p-channel transistor performances were less sensitive to grain boundaries.

## 1. Introduction

Si thin-film transistors (TFTs) have been attracting a great deal of attention because they can be applied to such devices as liquid crystal display drivers,[1] load transistors in static random access memory cells[2] and three-dimensional integrated circuits.[3] Required performance of TFTs include high carrier mobility and low source-to-drain leakage current. For specific applications, performances not only of n-channel transistors but also of p-channel transistors have to be high. One promising approach for achieving these performance requirements is to prepare Si films having large crystal grains. We have reported that solid phase nucleation of amorphous Si film deposited on $SiO_2$ can be enhanced at steps formed at the $SiO_2$ surface and, as a result, polycrystalline Si (poly-Si) films having large grain size can be formed.[4,5] Preliminary results obtained from n-channel TFTs have also been reported. This step-induced nucleation is very attractive for formation of poly-Si films for TFTs since it offers possibilities not only of controlling nucleation sites but also of acting as a stencil for crystal orientation alignment. In this work, we first investigate grain size and crystal orientations of the nucleation controlled poly-Si films. Next we report characteristics of both n- and p-channel TFTs fabricated on the Si films are investigated and compared with these of TFTs fabricated on Si films formed without nucleation control on flat substrates.

## 2. Experiment

The substrate used in this work were thermally oxidized $SiO_2$/Si substrates. Steps of a stripe pattern at the substrate surface were formed at the Si surface by the anisotropic etching of Si(100) wafer using a KOH: IPA : $H_2O$ (1:1:2) solution and thermal $SiO_2$ as etching mask. After removing the $SiO_2$ mask the Si wafers were oxidized to form the $SiO_2$/Si substrates with surface steps. The step height was set at about 100nm. These $SiO_2$/Si substrates were loaded into a vacuum chamber which has back ground pressure at about $1 \times 10^{-7}$Pa. Amorphous Si (a-Si) films were deposited by vacuum evaporation using an electron beam gun. Prior to deposition of a-Si, the substrates were heated at 450°C for 60min in order to clean their surface. Thickness of a-Si layer was about 100nm. After deposition, the a-Si/ $SiO_2$ /Si samples heated *in-situ* at 450°C for 60min in order to densify the deposited a-Si film. After removing the sample from the chamber, it was treated in a boiled mixture of $NH_4OH : H_2O_2 : H_2O$ (1:1:2). Solid phase crystallization was performed by annealing the sample at 600°C in an $N_2$ ambient.

In order to electrically characterize, n- and p-channel MOSFETs with Al gates were fabricated on the Si films. For the nucleation control, the anisotropically etched steps were fabricated at the source/drain edges of MOSFETs. For comparison, MOSFETs were also fabricated on Si films prepared without nucleation control on flat $SiO_2$/Si substrates. Prior to MOSFET fabrication, the samples were annealed at 1100°C for 60min in an $N_2$ ambient. The source and drain were formed by thermal diffusion at 900°C from a solid source. The gate oxide was formed by thermal oxidation at 1050°C and it's thickness was set at 100nm. The thickness of the active region was about 100nm.

# 3. Results and Discussion

*3.1 Crystallinity of Si films*

Figure 1 shows a bright-field TEM (transmission electron microscope) micrograph and a selected area diffraction pattern taken from a sample annealed at 600°C for 16 hours. We can see that the growth of polycrystalline Si grains from the step which resulted in formation of polycrystal Si zone along the step line. The diffraction pattern shows that the grain is ⟨111⟩ oriented in the surface normal direction although it contains twins. From the observation along the step line, it has been found that the vast majority of crystallites has ⟨111⟩ axis in the surface normal direction. Concerning the shape and the size of grains, the TEM dark field analysis has shown that grains are in the form of stripes. The typical size of grains was approximately 0.5$\mu$m in wide (along the step) and approximately 3$\mu$m in length (along the direction perpendicular to the step).

In order to investigate the in-plane crystal orientation, the angle of the twins with respect to the step were measured and compared with those of grains appeared randomly at the flat substrate region. It is well known that twins appear at (111) plane in Si crystal. Therefore we can determine the in-plane crystal direction from the observed angle of twins. Figure 2 shows distribution of twins in both grains grown from the step and grains grown randomly at flat region. The twins in the grains grown from the step mostly appeared at a peculiar angle(20−30° from the step line), while those in the randomly grown grains showed no peculiar angle distribution. These results show that the most of the nucleation-controlled grains tends to have its ⟨211⟩ axis in the direction perpendicular to the step. Two possible causes can explain the fact that twins in grains grown from the step tend to have peculiar angle. One is that twins originally appear at random direction but, as the growth proceeds, two adjacent grains conflict each other and the growth of one of them is stopped. The other is that in-plane orientation of grains is limited from the initial stage of the growth. Further investigations on this are in progress.

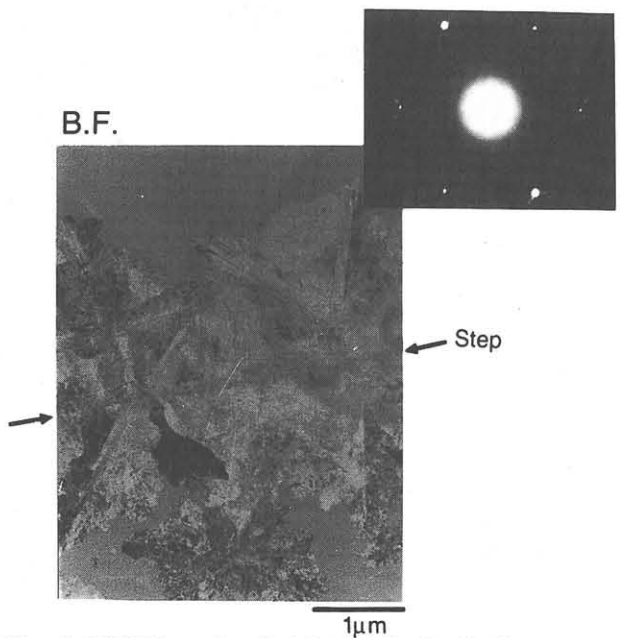


**Fig. 1** TEM top view(bright field) of a Si film annealed at 600°C for 16 hours, showing crystallization from the step. TED pattern is also shown, showing ⟨111⟩ orientation of crystallites.

*3.2 Characteristics of TFTs*

Figure 3 shows schematic cross-section of MOSFETs fabricated by utilizing the nucleation control. The steps for nucleation control were formed at the source/drain edges. Thus the growth of Si grains starts from both the source edge and the drain edge toward the center of the channel. Under the conditions used for the preparation of Si films, the growth length of Si grains from the step is limited to about 3$\mu$m by randomly nucleated grains at the central zone of the channel. The channel length of MOSFETs fabricated was 10$\mu$m. Therefore about 60% of the active

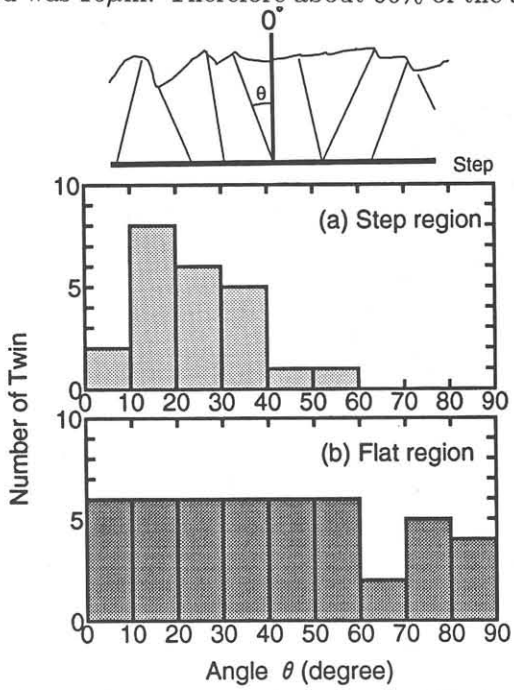


**Fig. 2** Angle distribution of twins appeared in Si grains grown from the step(a) and in grains grown randomly at the flat substrate region (conventional solid phase crystallization) (b).

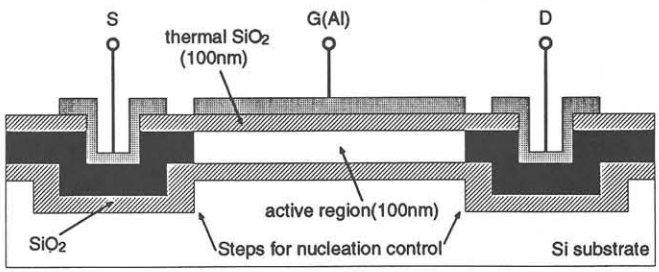


**Fig. 3** Schematic illustration of TFTs fabricated by utilizing the nucleation control by surface steps. The steps were formed at the source/drain edges.
W/L = 50$\mu$m/10$\mu$m. $t_{ox}$ = 100nm.

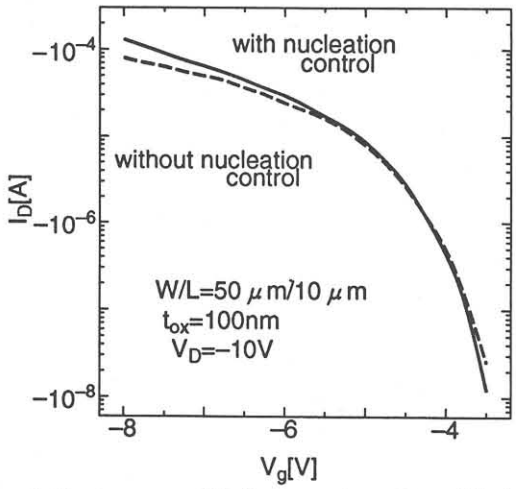


**Fig. 4** Drain-current($I_D$) vs. gate-voltage($V_G$) characteristics of p-channel TFTs fabricated on Si films prepared with nucleation control by using steps and without nucleation control (on flat substrates).

region was occupied by Si crystals grown from the steps (source and drain) and the rest at the central zone was occupied by randomly nucleated Si grains. In order to determine the effectiveness of the nucleation control process, MOSFETs were fabricated on Si films on $SiO_2$/Si substrates prepared under the same crystallization conditions.

Figure 4 shows comparison of drain-current vs. gate-voltage characteristics of p-channel MOSFETs fabricated on Si films prepared with nucleation control (stepped substrate surface at the source/drain edges) and without nucleation control (flat substrate). We can see that the nucleation control process is useful in improving TFT characteristics. In Table 1, the channel carrier mobility and the subthreshold slope obtained from n- and p-channel TFTs and MOSFETs fabricated on bulk Si(100) wafers are summarized. p-channel TFT fabricated by utilizing the nucleation control showed channel mobility $\mu_p \simeq 150\text{cm}^2/\text{Vs}$, which is about 3/4 of the value obtained from bulk MOSFETs and is twice of the value obtained from MOSFETs fabricated on Si films formed by the conventional solid phase crystallization(on flat substrate). The subthreshold slope is also improved by employing the nucleation control. On the other hand, more drastical differences in channel mobility between the materials have been observed for n-channel transistors. That is, n-channel MOSFETs fabricated by utilizing the nucleation control showed channel mobility $\mu_n \simeq 200\text{cm}^2/\text{Vs}$ which is about 2/5 of the value of bulk MOSFETs and is approximately one order higher than that of the MOSFETs fabricated without nucleation control. These results suggest that effects on TFT performance of grain boundaries are less for p-channel than for n-channel transistors. A possible cause is defect state density distribution at the grain boundaries.

# 4. Conclusions

Crystallinity of polycrystalline Si films formed by solid phase crystallization with nucleation control using surface steps and characteristics of TFTs fabricated on the Si films have been investigated. The followings summarize the present work.

1. The vast majority of Si grains grown from the step has ⟨111⟩ axis in the direction normal to the substrate surface.
2. Concerning in-plane orientation, ⟨211⟩ axis of the grains grown from the step tends to align in the direction perpendicular to the step line.
3. The application of the nucleation control by using surface step is effective in improving TFT performance for both n- and p-channels. The improvement is much pronounced in n-channel transistors.


1) A. Mimura, N. Konishi, K. Ono, J. Ohwada, Y. Hosokawa, Y. A. Ono, T. Suzuki, K. Miyata and H. Kawakami: IEEE Trans. Electron Devices **ED-36** (1989) 351.

2) K. Yuzuhira, K. Ichinose, T. Mukai, Y. Kohno, M. Shimizu, M. Inuishi and T. Matsukawa: *1989 Symp. VLSI Technology, Dig. Tech. Pap., Kyoto, 1989* (Business Center for Academic Societies of Japan, Tokyo, 1989) p. 61.

3) See, for example, *Ext. Abstr. 8th Int. Workshop on Future Electron Devices–Three Dimensional ICs and Nanometer Functional Devices* (R&D Association for Future Electron Devices, Tokyo, 1990).

4) T. Asano and K. Makihira: *Ext. Abstr. 1992 Int. Conf. on Solid State Devices and Materials, Tsukuba, 1992* (Business Center for Academic Societies of Japan, Tokyo, 1992) p. 29.

5) T. Asano and K. Makihira: Jpn. J. Appl. Phys. **32** (1993) 482.


**Table 1** Comparison of channel mobility and subthreshold slope of MOSFET fabricated on bulk Si, on Si film formed by the nucleation control by surface steps, and on Si films formed without nucleation control (conventional solid phase crystallization on flat substrates).

| | | bulk | TFT with Nucleation Control | TFT without Nucleation Control |
|---|---|---|---|---|
| p | mobility: $\mu_p$ ($\text{cm}^2/\text{V}\cdot\text{s}$) | 200 | 150 | 75 |
| | Subthreshold slope(mV/decade) | 250 | 400 | 500 |
| n | mobility: $\mu_n$ ($\text{cm}^2/\text{V}\cdot\text{s}$) | 500 | 200 | 15 |