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A Novel Model for Lowering of Grain-Boundary Potential Barrier in High Mobility Poly-Si TFTs

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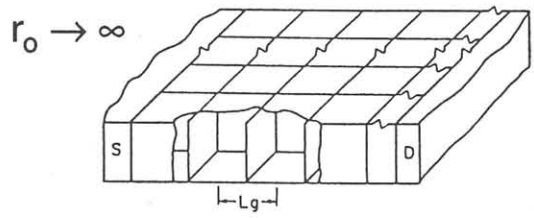
We propose a novel model for grain boundary where the grain is surrounded by a curved surface. A new equation for the potential barrier height is derived from this model. It is demonstrated that the potential barrier height greatly depends on the surface curvature of the grain boundary and rapidly lowers as the curvature radius decreases. This model is supported by high resolution TEM observations.

1. Introduction

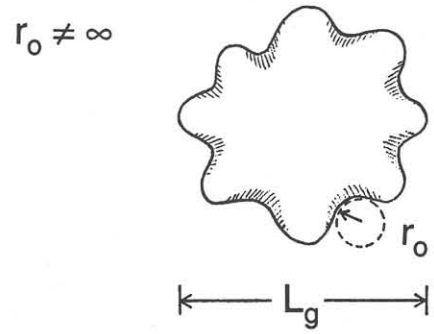
Poly-Si TFTs, especially those made from laser-annealed poly-crystallized Si films, have high mobility in spite of their polycrystalline structure containing many grain boundaries[1,2]. Poly-Si TFT electrical characteristics such as field effect mobility are strongly influenced by grain boundary properties rather than grain size. These properties are characterized by the potential barrier formed by trapped carriers at the grain boundary. The high mobility characteristics clearly show that the potential barrier height Φ_B at the grain boundary is very low. The potential barrier is generally calculated based on the model of grains surrounded by flat surface grain boundaries (flat surface G. B. Model) as shown in Fig. 1(a).[3] In this model, the curvature of the grain boundary r_o is nearly infinite and larger than the average grain size L_g. The model, however, cannot consistently explain Poly-Si TFT characteristics because a high potential barrier height is calculated from this model.

Figure 2 shows the relationship between carrier trap state density $N^*(cm^{-3})$ and carrier trap state surface density $N_{st}(cm^{-2})$ for sputtered Poly-Si TFTs and CVD Poly-Si TFTs. The value N_{st} was calculated from the potential barrier height by using the flat surface G. B. Model. On the other hand, N^* was calculated from subthreshold characteristics (S value), assuming that the distribution of the carrier trap state is uniform in the grain and grain boundaries. The relationship between N^* and N_{st} was derived as $N_{st}=N^*\cdot L_g/3$ from the flat surface G. B. Model in Fig. 1(a). Figure 2 shows that this relationship does not hold in both cases. This result suggests that the grain boundary surfaces are not flat and the geometrical structure of the grain boundaries seriously influence the potential barrier heights, that is , poly-Si TFT characteristics.

We propose a novel model for grain boundary that elegantly leads to lowering the potential barrier heights and explains the experimental results well.



(a) Flat surface grain boundary



(b) Curved surface grain boundary

Fig. 1 (a) Conventional and (b) newly proposed grain boundary models.

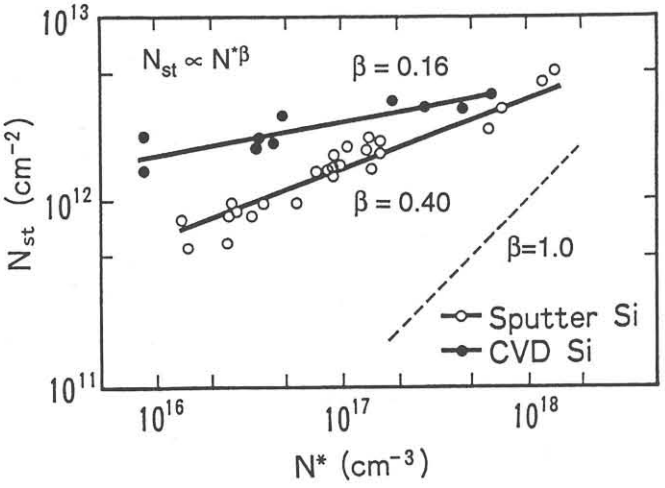


Fig. 2 Carrier trap state density N^* versus carrier trap state surface density N_{st}.

2. Curved Surface Potential Barrier Model

Figure 1(b) shows the newly proposed grain boundary model where grain is surrounded by a curved surface (*curved surface G. B. Model*). In this model, $r_o \neq \infty$ and $L_g > r_o$. We assumed that the curved surface has spherical or cylindrical surfaces having radii r_o. The potential barrier height Φ_B is derived from the following Poisson's equation.

$$\nabla^2\Phi(r) = \partial^2\Phi/\partial r^2 + (\alpha/r)\partial\Phi/\partial r = q(n + N_A) / \varepsilon_s \quad (1),$$

where $\alpha = 1$ is the cylindrical surface, $\alpha = 2$ is the spherical surface, q is the electronic charge, ε_s is the permittivity of Si, N_A is acceptor-type impurity, and n is the free electron density given by

$$n = C_{ox}(V_g - V_{th}) / qd.$$

Here, C_{ox} is the gate capacitance per unit area, $V_g - V_{th}$ is the effective gate voltage, and d is the inversion-layer depth.

In boundary conditions of $\Phi(r=0)=\Phi(r=\infty)=0$ and $(\partial\Phi/\partial r)_{r=0}=(\partial\Phi/\partial r)_{r=\infty}=0$, potential barrier height $\Phi_B(=\Phi(r=r_o) - \Phi(r=0))$ is given by the calculation based on eq.(1) for $V_g - V_{th}>0$ and using trapped charge density Q_s in grain boundary.

$$\Phi_B = q(n+N_A)r_o^2\{(1+\alpha^2Q_s^2/4q^2(n+N_A)^2r_o^2)^{1/2} - 1\}/\alpha^2\varepsilon_s \quad (2).$$

When the gate voltage is high , the free carrier density n is sufficiently higher than N_A, and the carrier trap states in the grain boundary surface with the density $N^*_{st}(cm^{-2})$ are nearly filled, then equation (2) is as follows.

$$\Phi_B = qnr_o^2\{(1 + \alpha^2N^{*}_{st}{}^2 / 4n^2r_o^2)^{1/2} - 1\} / \alpha^2\varepsilon_s \quad (3).$$

In $r_o \rightarrow \infty$, eq.(3) is equal to the potential barrier height of $\Phi_{Bo}=qN^{*}_{st}{}^2/8\varepsilon_s n$ derived from the flat G. B. Model.

3. Results and Estimates

Figure 3 shows the changes of Φ_B as a function of radius r_o in spherical and cylindrical surfaces. In both cases, Φ_B are lower than that in the flat G. B. Model. These barrier heights decrease especially rapidly for radii shorter than 50 nm. Moreover, the lowering of Φ_B is pronounced for the higher carrier trap state density N^*_{st}. Figures 4(a) and 4(b) show Φ_B versus gate voltage for cylindrical and spherical grain boundaries, respectively. The change of Φ_B relative to the gate voltage is larger in the cylindrical grain boundary than in the spherical grain boundary. It was found that the potential barrier height has a profound effect on the curvature in the grain boundary and lowers as the curvature radius decreases, especially in the spherical grain boundary. These results suggest that complicated grain boundary surfaces such as cylindrical or spherical surfaces lower the potential barrier.

Figure 5 shows a high resolution TEM photograph of the poly-Si film in the poly-Si TFT made from an Ar laser-irradiated sputtered a-Si film.[2] Very high mobility poly-Si TFTs were obtained from this poly-Si film. As shown in Fig. 5, the grain boundary consists of curved surfaces, not flat surfaces. The curvature of grains is several tens of nanometers. This curvature in

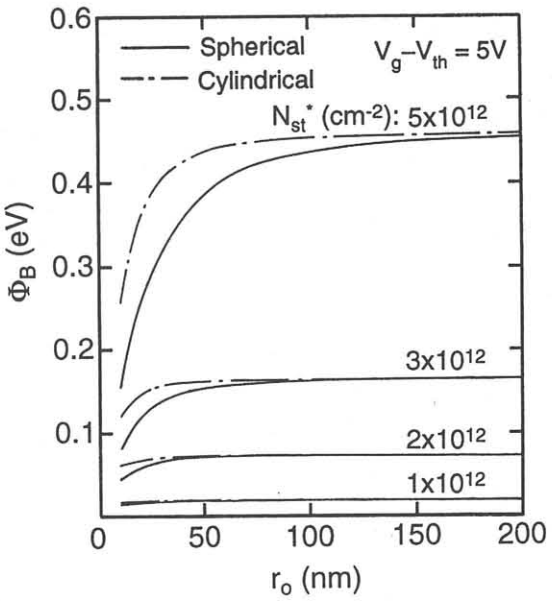


Fig. 3 Potential barrier height variations as a function of curvature radius r_o in spherical and cylindrical surfaces.

the grain boundaries leads to very high mobilities.

4. Conclusions

We have proposed a new curved surface G. B. Model instead of the conventional flat surface G. B. Model. We have demonstrated that the potential barrier height Φ_B of poly-Si TFTs strongly depends on the surface morphology of the grain boundary and rapidly lowers as the curvature radius of the grain boundary surface decreases. It was also found that this novel model is supported by high resolution TEM observations.

5. Acknowledgement

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References

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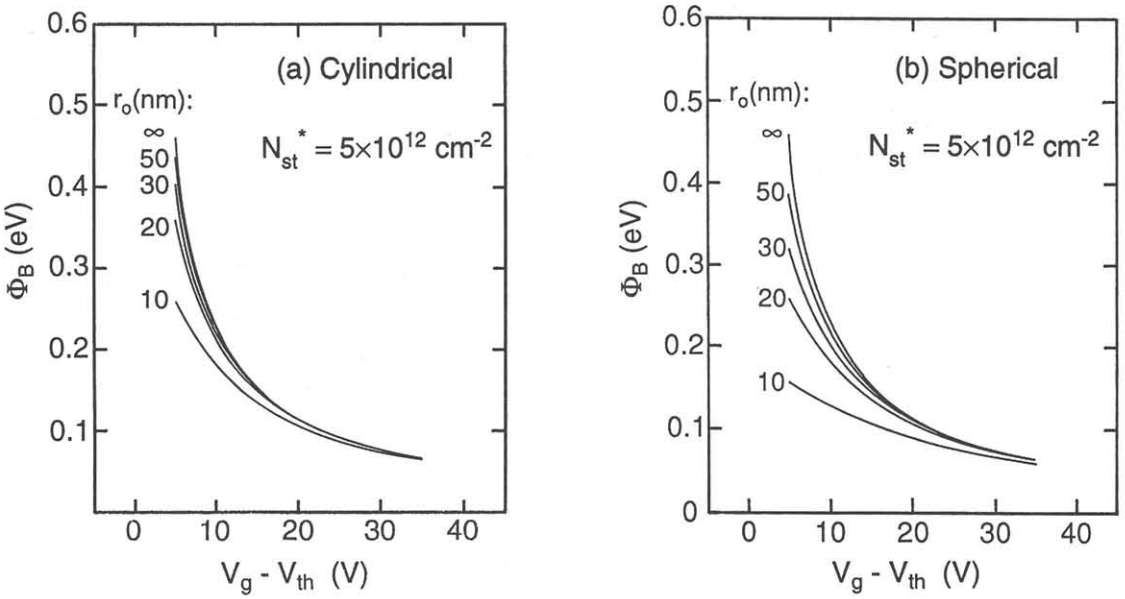

Fig. 4 Potential barrier height Φ_B versus gate voltage in (a) cylindrical and (b) spherical grain boundary.

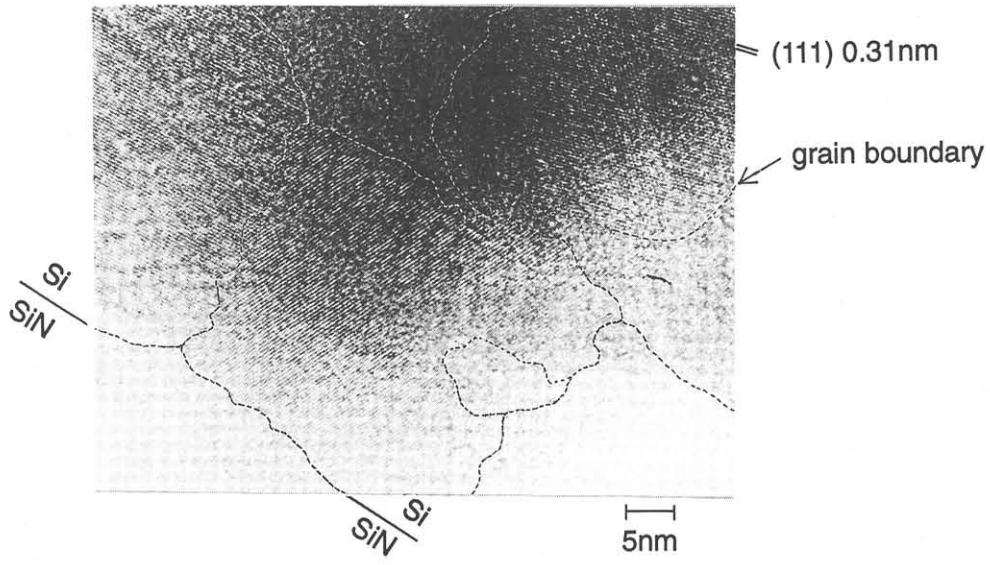

Fig.5 High resolution TEM photograph of the poly-Si film in high-mobility Poly-Si TFTs.