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Ti-Silicided Ultra Shallow p^+-n Junction Formation by As-Preamorphization through Pre-Deposited Amorphous Si Layer

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Major limiting factors in the linear scaling down of the shallow source/drain junction are the boron channeling effect and the Si consumption phenomena during the silicidation. We can approach to solve these problems using the As-preamorphization method through the pre-deposited amorphous Si layer. The pre-deposited amorphous Si layer made the junction depth shorten as much as the thickness of the layer and was effectively utilized for the consuming Si source during Ti silicidation. This method was practically applied to fabricate the PMOSFET(W/L=20/0.3μm) through the SES(selectively etched Si) technology.

1. INTRODUCTION

For the deep submicron device, the linear scale down of the junction depth is difficult. One reason is the limitation in the formation of the ultra shallow junction because of the boron channeling[1] and its high diffusivity. Another reason is the Si consumption phenomena occurred during the silicidation which can result in the excessive leakage current[2]. One way to eliminate the boron channeling is to preamorphize the Si substrate prior to the boron implantation[3]. Also, it is known that the As-preamorphization with the relatively low dose less than $4\times10^{14}cm^{-2}$ can suppress effectively the boron channeling and the good electrical characteristics can be obtained[4,5]. In this experiment, by adding the As-preamorphization through the pre-deposited amorphous Si(a-Si) layer of 600Å, we have found that the channeling of 10keV B^+ ions is avoided and the much shallower p^+-n junction depth can be obtained. That is, the junction depth is shortened as much as the thickness of the pre-deposited a-Si layer keeping the boron peak at the Si surface. Another main advantage is that the pre-deposited a-Si layer can be utilized for the Si consumption occurred during Ti silicidation.

2. EXPERIMENTALS

In the previous experiment[4,5], it is verified that the As^+ implantation with a dose of $2\times10^{14}cm^{-2}$ is enough to preamorphize the Si layer in order to avoid the channeling of B^+ ions implanted with an energy of 10keV.

In this experiment, in order to reduce the p^+-n junction depth much more for the given B^+ implantation conditions and locate the boron peak near the Si surface, an amorphous Si layer of 600Å thickness was deposited by LPCVD method on the Si surface before As-preamorphization. And the preamorphization of the single crystal Si surface layer under the pre-deposited a-Si layer was performed by As^+ implantation. As-preamorphization dose was fixed at $2\times10^{14}cm^{-2}$ and the energy was varied from 60keV to 75keV. Subsequently, B^+ ions were implanted at a dose of $1.5\times10^{15}cm^{-2}$ with an energy of 10keV. Generally, the shallow junction needs the silicide layer in order to reduce the sheet resistance. By the way, the silicidation results in the Si consumption as much as nearly the thickness of the silicide layer. This induces the reduction of the distance between the silicide/Si interface and the junction interface or locally the schottky diode characteristics due to the shortening of the two interfaces. As a result, the junction leakage current occurs excessively. Fortunately, in our work, the pre-deposited a-Si layer can be utilized for the consuming Si source during silicidation. In order to practically apply the above method for the MOSFET fabrication, it is necessary to remain the a-Si layer selectively only on the source/drain area with self-aligned method. For this, we have developed the new processing technology named with the SES(selectively etched Si).

The key process steps are such as the gate patterning with PSG layer, the photoresist etch-back, the selective a-Si etching by RIE and PSG layer wet etching, etc. To this structure, Ti film of about 400Å was deposited by sputtering. Then, silicidation and selective Ti etching were performed.

Using the above methods, the PMOSFET with 0.3μm gate length was fabricated. The photolithography process was done by the 'mix-and-match' method using the direct e-beam and stepper.

3. RESULTS AND DISCUSSIONS

Fig.1 shows the depth profiles of the as-implanted borons in the samples fabricated using above method. As shown in the figure, the boron channeling in the samples using both the pre-deposition of a-Si layer and the As-preamorphization(profiles 'c' 'd' 'e' & 'f') is suppressed more than that of the borons implanted into the sample without the As-preamorphization(profile 'b'). The channeling is reduced more and more as the As implant energy increases. For the comparison, the profile of the borons implanted into only the single crystal Si(profile 'a') is included. We can see that the effective junction depth of the as-implanted borons in the sample preamorphized with As/75keV is about 50nm for the background concentration of $1\times10^{17}cm^{-3}$.

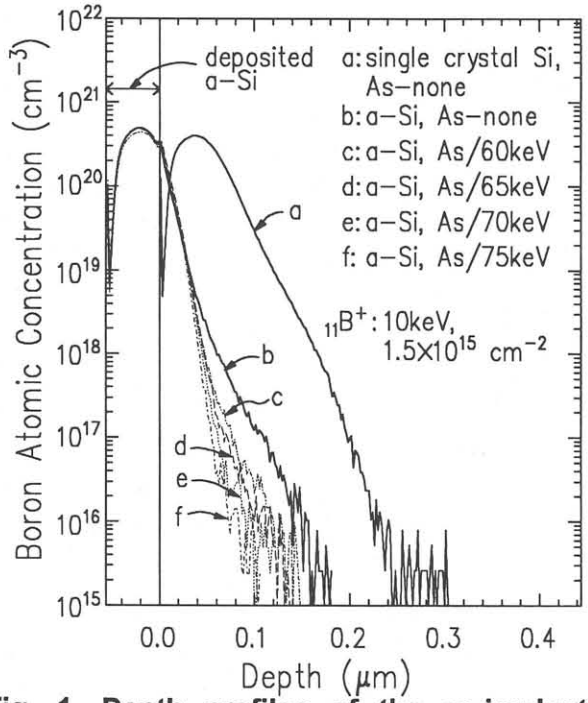

Fig. 1. Depth profiles of the as-implanted boron atoms with As-preamorphization energy.

Fig.2 shows the depth profiles of the B and As annealed with different RTA temperatures in the samples preamorphized with As/75keV/2× $10^{14}cm^{-2}$. All As profiles are within the boron profiles, so that the implanted As atoms would not affect the junction characteristics. For the all RTA temperatures, the junction depth was about 0.13 to 0.16μm range. As shown, the junction depth was considerably increased during RTA and especially, the abnormal enhanced diffusion was occurred at 1050°C.

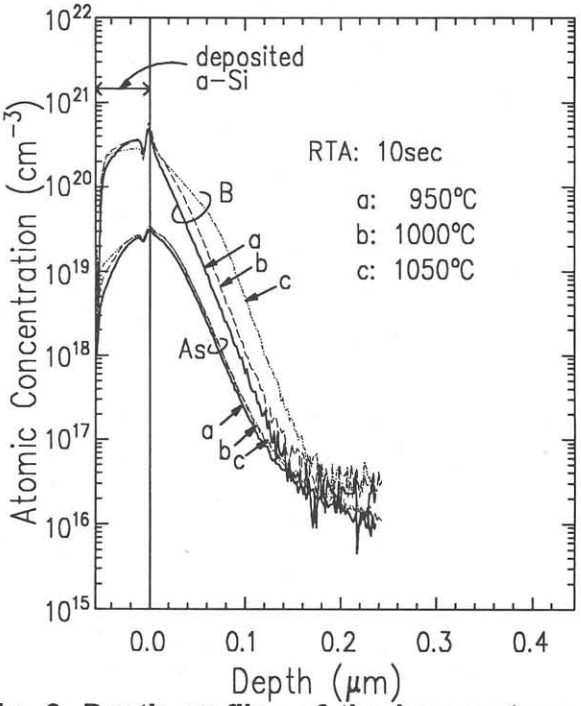

Fig. 2. Depth profiles of the boron atoms in the samples annealed with RTA.

Fig.3 shows the I-V characteristics of the p^+-n diode silicided using the pre-deposited a-Si layer remained only on the active area as the consuming Si source. Ti silicidation was performed with two steps, in which the first step was 650°C/30sec and the second 850°C/20sec for the as-deposited Ti film of about 400Å. The resultant thickness of the Ti silicide layer was about 800Å. In the Fig.3, we can see that the leakage current increases as the As implant energy increases. This is because the distance from the silicide/Si interface to the junction reduces as the junction depth becomes shallower(from 'a' to 'd'). Curve 'd' in Fig.3 corresponds to the case silicided right after removing the pre-deposited a-Si layer, in which the leakage current increases excessively.

From the results, we can say that the a-Si layer is used effectively for the consuming Si source during the silicidation.

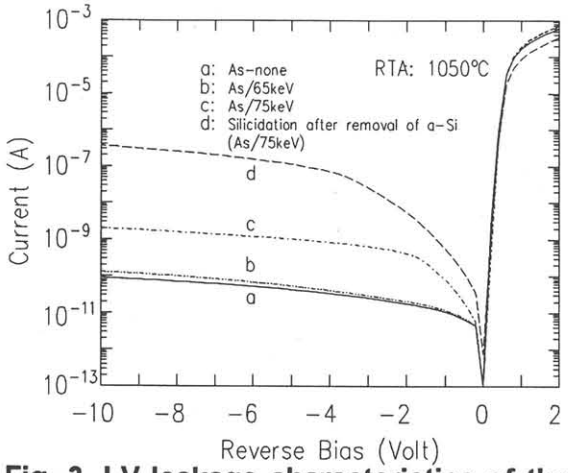

Fig. 3. I-V leakage characteristics of the p⁺-n diode used the pre-deposited a-Si layer as the consuming Si source during Ti silicidation, except(d).

The schematics in order to practically apply the above method for the PMOSFET fabrication are shown in Fig.4. And the SEM cross section view of the gate structure fabricated with this technology is shown in Fig.5. Side-wall oxide was the conventional APCVD oxide.

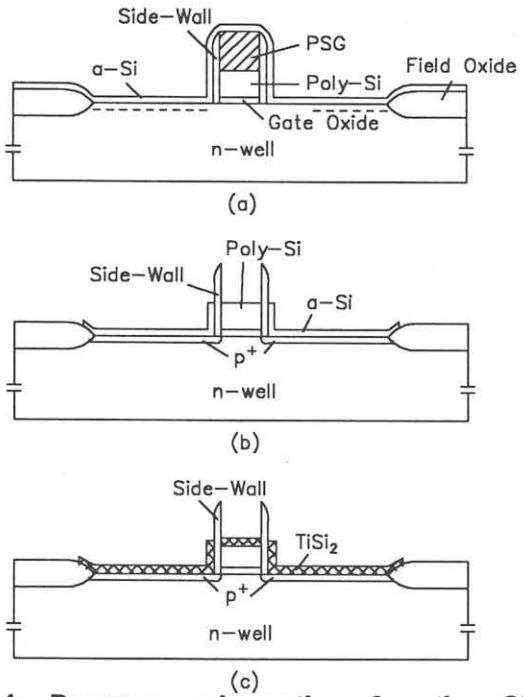

Fig. 4. Process schematics for the SES technology: (a) PSG deposition, gate patterning, side-wall formation, a-Si deposition, implantation, (b) PR coating & etch-back, a-Si etching, (c) Ti silicidation.

Finally, the I_D-V_D characteristics of the PMOSFET with the Ti-silicide layer formed by using the SES structure is shown in Fig.6. The gate layout dimensions for the direct e-beam was the gate length of 0.3μm and the width of 20μm.

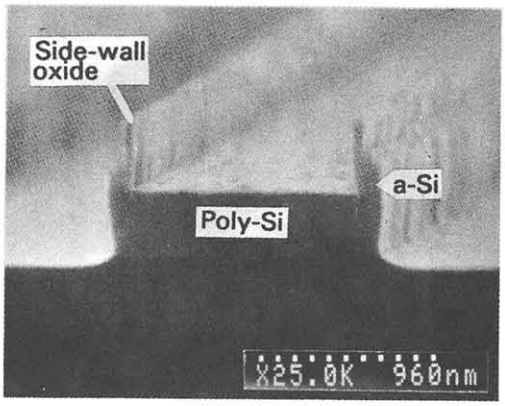

Fig. 5. The SEM cross-section view of the gate structure fabricated with the SES process.

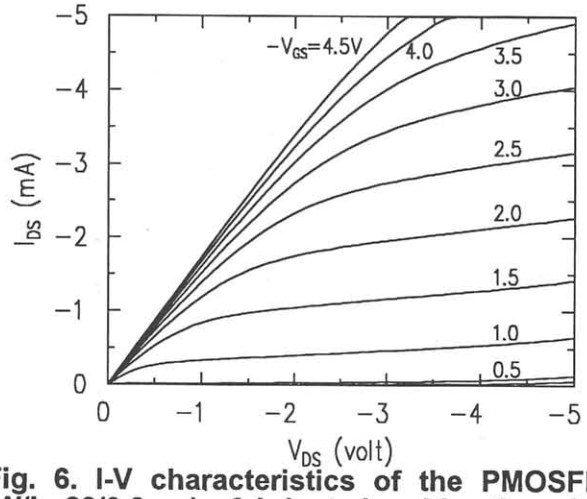

Fig. 6. I-V characteristics of the PMOSFET (W/L=20/0.3μm) fabricated with the SES technology.

4. CONCLUSIONS

We can conclude that the method of As-preamorphization through the pre-deposited a-Si layer is effective for the formation of the ultra shallow junction and also suitable for the application of the silicidation to the shallow junction without inducing much leakage current. In reality, the SES technology makes it possible to apply the above method practically to the PMOSFET.

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