Extended Abstracts of the 1993 International Conference on Solid State Devices and Materials, Makuhari, 1993, pp. 119-121

Growth of GaAs on Si(100) with $(GaAs)_{1-x}(Si_2)_x$/GaAs Strained-Layer Superlattice by Migration-Enhanced Epitaxy

Kazuhiko Nozawa, Tatavarti Sudersena Rao* and Yoshiji Horikoshi

NTT Basic Research Laboratories
Musashino-shi, Tokyo 180 Japan

*Current address: Institute of Microstructural Sciences, National Research Council of Canada, Otawa, Canada.

$(GaAs)_{1-x}(Si_2)_x$/GaAs strained-layer superlattices (SLS) have been used as buffer layers to reduce the dislocation density in GaAs on Si grown by migration-enhanced epitaxy. $(GaAs)_{1-x}(Si_2)_x$ layers relax little, even at high growth temperatures (~500°C) compared with $In_xGa_{1-x}As$, which is a constituent of conventional SLSs. Cross-sectional transmission electron microscopy investigations revealed extensive threading dislocation bending at the $(GaAs)_{1-x}(Si_2)_x$/GaAs SLSs. Etch-pit density measurements indicated average dislocation densities of ~5×10^5 cm^{-2}, more than half an order of magnitude lower than for samples with ordinary $In_xGa_{1-x}As$/GaAs SLSs. The $(GaAs)_{1-x}(Si_2)_x$/GaAs SLS is thus more promising for reducing the dislocation density in GaAs grown on Si at high temperatures than are conventional SLSs, such as $In_xGa_{1-x}As$/GaAs.

1. Introduction

The heteroepitaxial growth of GaAs on Si substrates (GaAs/Si) has attracted much attention in recent years because of its potential for integrating Si- and GaAs-based device structures. In previous papers[1-3], we demonstrated that low-temperature (300°C) migration-enhanced epitaxy (MEE) growth can produce very low dislocation density (~7×10^4 cm^{-2}) GaAs/Si with the aid of an $In_{1-x}Ga_xAs$/GaAs strained-layer superlattice (SLS). However, an important problem is that annealing at temperatures above 450°C increases the dislocation density. This is partially due to strain relaxation of the SLS.

Recently, pseudobinary alloys $(GaAs)_{1-x}(Si_2)_x$ were successfully grown by MEE on GaAs (100) substrates in the range of $0<x<0.25$.[4] We also found that the alloys are promising materials for an SLS buffer layer for overcoming the aforementioned problem.[5]

In this paper, we report preliminary results on the characteristics of those alloys and their application as an SLS buffer layer for GaAs/Si, although high quality alloys can be grown only at substrate temperatures above 500°C at this stage.

2. Experimental

A three-chamber MBE system was employed to grow the GaAs and the $(GaAs)_{1-x}(Si_2)_x$ alloys. During the GaAs growth in the MEE mode, the Ga and As_4 beam shutters are opened alternately. In the $(GaAs)_{1-x}(Si_2)_x$ alloy growth, conventional PBN effusion cells were used for Si beam generation. Because of the low Si beam flux and the relatively high growth temperature (~530°C) the As_4 beam shutter opening was made to coincide with the Si deposition so as to suppress the re-evaporation of As_4. The alloy composition was varied by changing the shutter opening time for the Si cell.

In a preliminary experiment, we grew the $(GaAs)_{1-x}(Si_2)_x$ alloy layers on GaAs (100) substrates. The growth of these layers has been reported in detail elsewhere.[4]

For the study of GaAs/Si growth, we used 3-inch Si (100) substrates with off-orientations of 2° toward the [011] direction. The details of the MEE growth and of the substrate preparation have been described elsewhere.[1,2] A standard two-step growth procedure was employed for these samples. The layer structure is shown in Fig. 1. We inserted 3 SLS packets of 5-periods of $(GaAs)_{1-x}(Si_2)_x$/GaAs, with x=0.2,where the $(GaAs)_{0.8}(Si_2)_{0.2}$ layer is 20nm thick and the GaAs is about 17nm. Before growth, the Si substrate was heated at 1000°C for 15 min to remove the surface oxide layer and to form a single-domain surface structure. After the substrate was cooled to 300°C, a 100-nm-thick GaAs layer was grown by MEE to serve as a initial nucleating buffer layer. This was followed by a 15 min annealing at 580°C. Then, the GaAs layers and three SLS packets of 5-period $(GaAs)_{0.8}(Si_2)_{0.2}$/GaAs were grown at 520°C by MEE (Fig. 1). The top GaAs layer of 3.0 μm was grown by either MBE (at 580°C) or MEE (at 530°C). The total film thickness was about 4 μm for all GaAs/Si samples. For comparison, GaAs/Si samples with conventional $In_xGa_{1-x}As$/GaAs SLSs were also prepared. Here, it should be noted that the present SLS parameters, such as the Si percentage, thickness and period, have not been optimized.

For these samples, the x-ray diffraction was measured with a high-resolution double-crystal x-ray diffractometer. Some of the samples were also examined by transmission electron microscope (TEM) and etch-pit density (EPD) observations. The EPD was determined by Nomarski optical microscopy for samples etched in molten KOH for 4 min at 350°C.

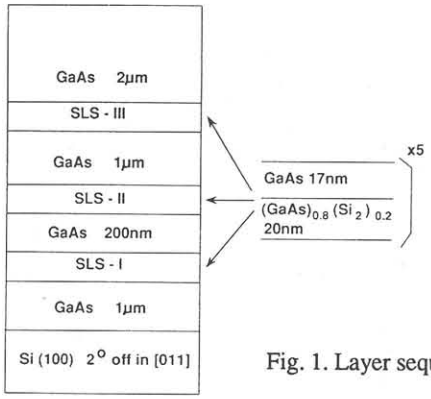

Fig. 1. Layer sequence.

3. Results and Discussion

First, we report preliminary results on the characteristics the $(GaAs)_{1-x}(Si_2)_x$ alloys. Structural analysis of the $(GaAs)_{1-x}(Si_2)_x$ layers indicated a single-crystal zincblende structure with no evidence of phase separation. The lattice constant of the alloys decreased nearly linearly with increasing Si content, in good agreement with Vegards rule (Fig. 2). In conventional SLSs, the typical mismatch between the constituent materials is about 0.5 to 1%. The mismatch of the $(GaAs)_{1-x}(Si_2)x$ alloy to GaAs is about 0.8% for x of

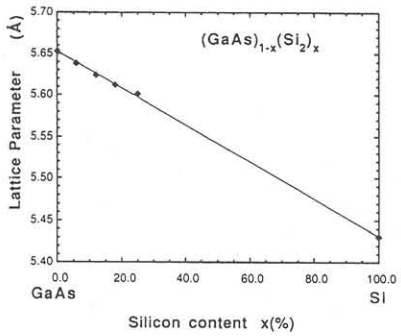

Fig. 2. Measured variation in lattice constant for $(GaAs)_{1-x}(Si_2)_x$ alloys as a function of x.

about 0.2. Double-crystal X-ray diffraction rocking curve measurements and cross-sectional TEM microscopy studies on a 10-period $(GaAs)_{0.8}(Si_2)_{0.2}$/GaAs SLS grown on a GaAs substrate[4] indicate sharp and abrupt interfaces of high crystalline quality. The $(GaAs)_{1-x}(Si_2)_x$/GaAs SLS, therefore, can be used as buffer layers to reduce the threading dislocation density in GaAs/Si.

Figure 3 shows the relationship between misfit strain and lattice mismatch for 500 nm of $In_xGa_{1-x}As$ and $(GaAs)_{1-x}(Si_2)_x$ grown on GaAs (100) substrates at 500°C. The lattice mismatch was calculated from x as determined by SIMS measurements, while the misfit strain was obtained from x-ray diffraction measurements. With increasing Si or In content, x, the misfit strain increases in proportion to the lattice mismatch, as shown by the dashed line in Fig. 3, if the misfit is accommodated not by misfit dislocation generation but only by elastic deformation. Therefore, if the strain is relaxed by generation of misfit dislocations, the strain should be lower than that shown by the dashed line in the figure. The figure shows that the $(GaAs)_{1-x}(Si_2)_x$ alloys are not relaxed in the range of $0<x<0.25$, probably because of the relatively strong Si-

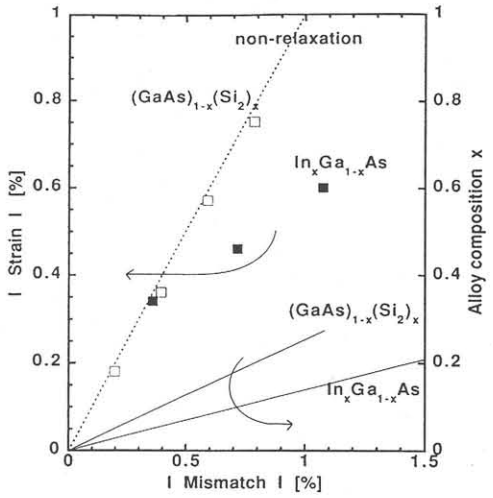

Fig. 3. Residual strain of $(GaAs)_{1-x}(Si_2)_x$ and $In_xGa_{1-x}As$ alloys as a function of lattice mismatch.

Si covalent bond. On the other hand, strain relaxation seems to occur in case of $In_xGa_{1-x}As$, where the misfit is larger than 0.1%. As pointed out in our previous reports,[2] low-temperature (~300°C) grown $In_xGa_{1-x}As$/GaAs SLSs are hardly relaxed in the range of $0<x<0.3$, but high-temperature (~580°C) grown $In_xGa_{1-x}As$/GaAs SLSs easily relax when $x>\sim0.1$. The present results, therefore, indicate that the $(GaAs)_{1-x}(Si_2)_x$/SLS is more promising than conventional SLSs such as $In_xGa_{1-x}As$/GaAs, as the $(GaAs)_{1-x}(Si_2)_x$ hardly relaxes, even at high growth temperatures.

It has also been suggested that a very effective way of decreasing the dislocation density is to use SLSs in which the constituent materials not only differ in strain but also have a substantial difference in elastic stiffness constants.[6] In this way it may be possible to deflect threading dislocations by using both strain and the elastic shear modulii of the individual layers. In such a situation, even when the strain in the layer is decreased and becomes less effective, the repulsion of the dislocations arising from the shear modulus mismatch remains unaffected. This is another reason for use of the alloy. The strong Si-Si covalent bond is expected to make the elastic stiffness constant (or shear modulus) of $(GaAs)_{1-x}(Si_2)_x$ be higher than for any III-V compound. We adopted the $(GaAs)_{1-x}(Si_2)_x$/GaAs SLS for the buffer layers to reduce the threading dislocation density in GaAs on Si. Next, the results of applying the SLS will be discussed.

Figure 4 shows a typical cross-sectional TEM micrograph near SLS-I and SLS-II in a GaAs/Si sample with three packets of $(GaAs)_{0.8}(Si_2)_{0.2}$/GaAs SLS layers grown by MEE at a temperature about 520°C. The threading dislocation density was very high at the GaAs and Si interface, and the SLS-I indeed blocked or deflected a large number of dislocations. It is clear from the picture that SLS-II, placed about 0.2 μm above SLS-I, deflected a major part of the remaining threading dislocations. A linear dislocation density count revealed that there is at least a factor of 100 difference in the dislocation densities for the areas below and above SLS-II. SLS-III, which is placed about 1.0 μm above SLS-II and is out of sight in this picture, prevented almost all of

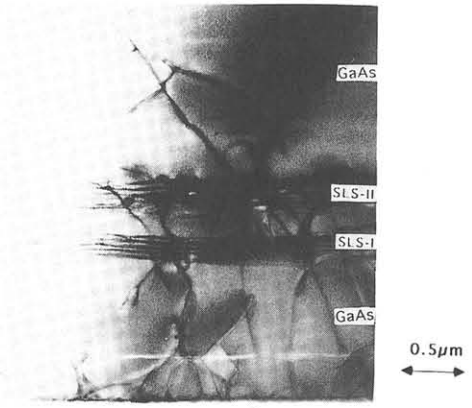

Fig. 4. Cross-sectional transmission electron micrograph of GaAs on Si grown with 3 packets of $(GaAs)_{1-x}(Si_2)_x$/GaAs SLS buffer layers. Each of the SLSs consists 5 periods of 20nm-$(GaAs)_{0.8}(Si_2)_{0.2}$ and 17nm-GaAs.

the threading dislocations from propagating to the surface, and the top 2.0 μm of GaAs is dislocation free in the areas investigated by TEM. The majority of these bent dislocations were found to run along the $(GaAs)_{1-x}(Si_2)_x$/GaAs interface for hundreds of microns.

Plan-view TEM studies indicated dislocation densities of less than $5x10^5 cm^{-2}$ near the surface. However, it becomes more difficult to determine the threading dislocation density as the density decreases, since TEM information, which only covers a small area, does not guarantee the uniformity of dislocation distribution for a wide range of TEM specimens. The EPD has been shown to be on the same order as the dislocation density observed by TEM, with no significant difference between them. Therefore, we also measured EPD for the samples and regard it as the threading dislocation density in this paper.

The EPD for each sample was estimated by observing three randomly chosen 100x100 μm squares on each 3-inch wafer. Etched surfaces of typical samples with a $(GaAs)_{1-x}(Si_2)_x$/GaAs SLSs are shown in Fig. 5. The two surfaces in the figure represent the minimum and the maximum EPDs, $3.33x10^5$ cm^{-2} and $8.84x10^5$ cm^{-2}. The average EPD was $5.63x10^5$ cm^{-2}. For comparison, the EPDs of samples with conventional $In_xGa_{1-x}As$/GaAs SLSs were measured.

There are at least two ways to control the built-in strain in SLS. One is to vary the In content, and another is to change the GaAs and/or InGaAs thickness. In this study, the former method was adopted so as to allow direct comparison with $(GaAs)_{0.8}(Si_2)_{0.2}$/GaAs SLS of identical layer structure. The calculated In content, x, was about 0.1, which gives the same lattice mismatch as that of the $(GaAs)_{0.8}(Si_2)_{0.2}$ alloy to GaAs. The respective minimum and maximum EPDs were $1.69x10^6$ cm^{-2} and $8.42x10^5$ cm^{-2} (Fig. 6). The average EPD was $1.30x10^6$ cm^{-2}, clearly demonstrating that EPD for samples with the $(GaAs)_{1-x}(Si_2)_x$/GaAs SLSs is more than half an order of magnitude lower than that of samples with typical $In_xGa_{1-x}As$/GaAs SLSs.

We believe the observed highly effective dislocation blocking is due to a combined effect of built-in strain in the SLSs and the relatively high elastic stiffness constant

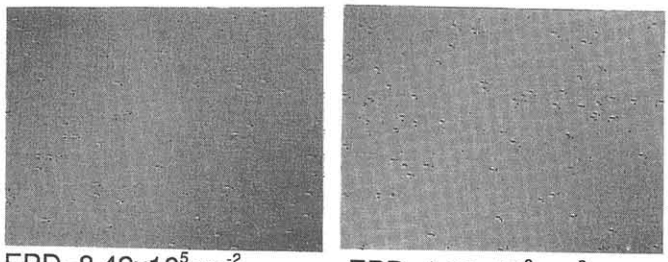

Fig. 5. Typical etched surfaces of the sample with $(GaAs)_{0.8}(Si_2)_{0.2}$/GaAs SLSs.

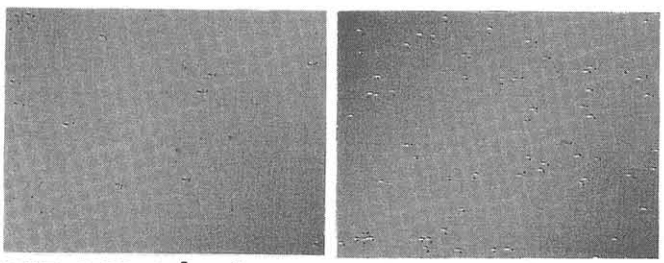

Fig. 6. Typical etched surfaces of the sample with $In_{0.1}Ga_{0.9}As$/GaAs SLSs.

of $(GaAs)_{1-x}(Si_2)_x$ alloys, because the strong Si-Si covalent bonding makes the shear modulus of Si higher than that of any III-V compounds. The use of the $(GaAs)_{1-x}(Si_2)_x$/GaAs SLS will open the way for suppressing strain relaxation even for low-temperature grown GaAs/Si heated after growth, although optimization for low-temperature growth of $(GaAs)_{1-x}(Si_2)_x$ is still needed.

4. Summary

A new SLS system of $(GaAs)_{1-x}(Si_2)_x$/GaAs was used as buffer layers to reduce the threading dislocation density in GaAs on Si grown by MEE. $(GaAs)_{1-x}(Si_2)_x$ layers grown on GaAs substrate hardly relax, even at high growth temperatures (~500°C) compared with $In_xGa_{1-x}As$, which is a constituent of the conventional SLS. Cross-sectional TEM investigations revealed extensive threading dislocation bending at $(GaAs)_{1-x}(Si_2)_x$/GaAs SLSs. EPD measurements indicated average dislocation densities of $5x10^5$ cm^{-2}, more than half an order of magnitude lower than that of samples with ordinary $In_xGa_{1-x}As$/GaAs SLSs. The $(GaAs)_{1-x}(Si_2)_x$/GaAs SLS holds greater promise for reducing the dislocation density in GaAs on Si than conventional SLSs, such as $In_xGa_{1-x}As$/GaAs, at high growth temperatures.

References

1) K. Nozawa and Y.Horikoshi; Jpn. J. Appl .Phys.**30** (1991) L668.
2) K. Nozawa and Y. Horikoshi; J. Electron. Mater. **21** (1992) 641.
3) K. Nozawa and Horikoshi; Jpn. J. Appl .Phys. **33** (1993) 642.
4) T. Sudersena Rao, K. Nozawa and Y. Horikoshi; Jpn. J. Appl. Phys. **30** (1991) L547.
5) T. Sudersena Rao, K. Nozawa and Y. Horikoshi; Appl. Phys. Lett. **62** (1993) 154.
6) R. I. Taylor; Solid State Tech. **4** (1989) 612.