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High Temperature Quantum Effect Devices Using InAs/AlGaSb Heterostructures

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We report electrical characteristics of InAs/(AlGa)Sb quantum wire devices based on deep mesa-etched structures with split gate. Quantized conductance has been observed at 80K for the first time. Observation of quantized conductance at such high temperatures become possible by the strong lateral confinement of electrons by the deep mesa-etching as oposed to simple planar split-gate approach together with the relatively high subband energy separation due to the small electron effective mass in InAs. Three types of quantum wire devices with different lateral wire-widths have been examined to yield quantum-effect observable temperature which is consistent with calculation results assuming 3000Å of highly resistive region.

1.Introduction

There have been extensive amount of work on the quantum wire transport mostly on (AlGa)As/GaAs hetrostructures[1-2] and on silicon based materials[3]. However, all these phenomena were observed at 4.2K or much lower temperatures. InAs quantum-effect devices[4] are potentially superior to the GaAs counterpart[5] in high temperature operation for their higher low-field mobility[6-8], higher conduction band discontinuities, and higher energy separation of sublevels. Because of this strong confinement nature and the low effective mass of electrons in the InAs well, quantum effects of the confined electron systems are expected to be observed at relatively high temperatures[4]. However, there have only been results measured at much lower temperatures than expected for several reasons[9-10]. In this paper, we report the fabrication and characterization of deeply etched quantum wires on an (AlGa)Sb/InAs heterostructure with split-gate by utilizing electron beam lithography and wet-chemical etching. In order to avoid the inherent gate leakage current in heterostructures based on antimonides, deeply etched wire structures have been investigated. Such devices with three different wire width will be investigated.

2.Experimental

The heterostructures have been grown by molecular beam epitaxy using ANELVA MBE-620 system. The growth techniques of the InAs/(AlGa)Sb are similar to what has been used to fabricate high performance heterojunction field-effect transistors[11-12].

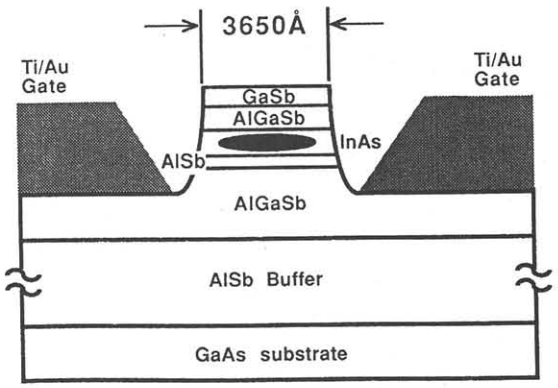

Figure 1. Schematic diagram of the InAs quantum wire structure with split-gate (sample B).

The heterostructure of device A, B, and C are quite similar with each other. As an example, structure of device B is shown in Fig.1, consisting of 2000Å of GaAs layer grown on undoped GaAs substrates, 1.0 μm AlSb buffer layer, 2000Å $(Al_{.5}Ga_{.5})Sb$ buffer layer, 70Å of AlSb layer, 150Å of InAs, 150Å of $(Al_{.5}Ga_{.5})Sb$, and 100Å of GaSb cap layer. The inserted 70Å of AlSb was intended to prevent leakage currents through (AlGa)Sb buffer layer which becomes appreciable at high temperatures under high gate bias voltages. In the structure A, major difference is that AlSb buffer layer is replaced by GaSb which is conductive and eventually limits gate voltage window. Lateral structure is defined by electron beam lithography and wet chemical etching with phosphoric-asid-based etchant and photoresist developper as a selective etchant

for antimonides[13]. Fabrication of deeply etched quantum wire structures using electron beam lithography and wet chemical etching is similar to what has been used to make ungated quantum wires[14]. Ti/Au was used as non-alloyed ohmic metal which is directly deposited on InAs layer after selective etching of antimonides. The nominal etch-depth were 1500Å. The JEOL multipurpose Scanning Electron Microscope system, JSM840A, was used as the electron beam source. The width of the devices, "A", "B", "C" were determined to be approximately, 4600Å, 3650Å and 8300Å, respectively by measuring the SEM and AFM images.

The conductance of the devices have been measured using HP4145B semiconductor parameter analyser. Voltage of only one of the split-gate was modulated reletive to the other end of the split-gate which is connected to the common ground and source terminal. This configuration was chosen to keep as much gate voltage range without suffering from gate leakage current. The drain voltage is set to 50mV (sample C) and 100mV (sample A and B). The conductance measurement errors were evaluated to be negligibly small when the drain voltage is less than ≈180mV. The effect of high drain voltage on the conductance quantization and drain current quantization will be reported elsewhere.

3.Results

The carrier concentration and the electron mobility of sample B measured at 77K by van der Pauw meathod were $1.07 \times 10^{12} cm^{-2}$ and 20,200 cm^2/Vs, respectively. The devices can be regarded as quasi-ballistic since the mean free path of each device is comparable to each wire length of each device. A clear quantized conductance of one to two fold multiples of $(2e^2/h)$ has been obtained for sample A as shown in Figure 2. It was only measured at 4.2K because severe leakage current broblem made it useless to measure at elevated temperatures due to conducting GaSb substrate. Besides, severe gate leakage current only allowed narrow gate voltage window of (-1.5V to +1.0V) to observe the conductance modulation.

On the other hand, sample B and C have structures which suffer less from leakage problems. As a result, application of wider range of gate voltages became possible in structures B and C. A clear quantized conductance steps of three to five fold multiples of $(2e^2/h)$ were observed at 80K with the sample B as shown in Figure 3. Clear conductance steps were observed at 114.8K. However, the conductance values at steps at those higher temperatures do not agree with multiples of $(2e^2/h)$. This is probably due to the parasitic MESFET which turns on very weakly at high temperatures. Figure 3 shows that the

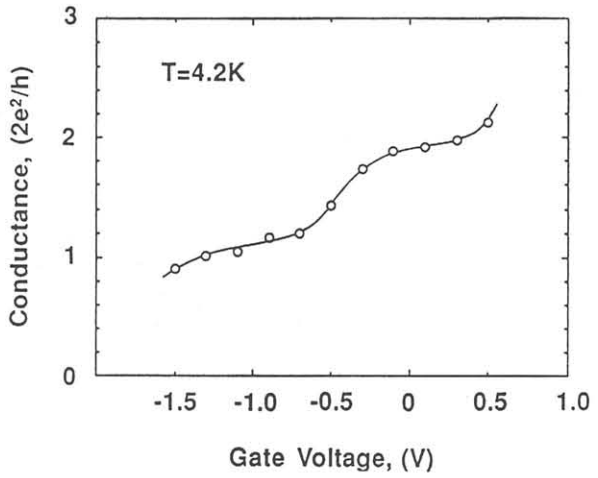

Figure 2. Conductance versus gate voltage of sample A. The nominal width of the wire is 4600Å.

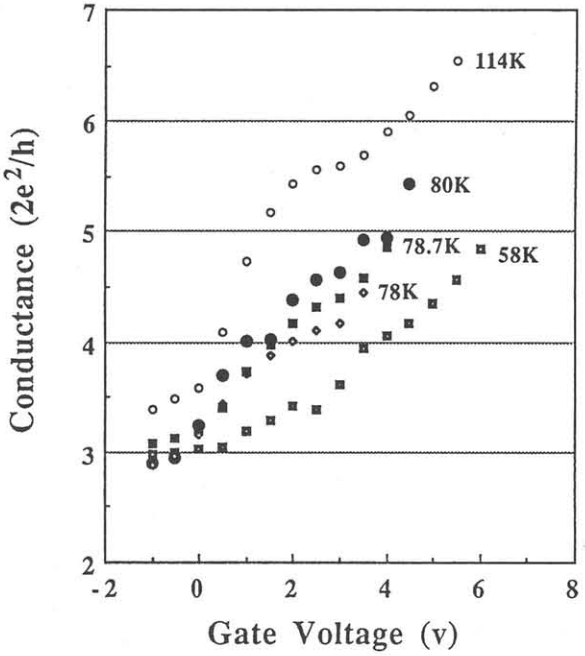

Figure 3. Conductance versus gate voltage of sample B. The nominal width of the wire is 3650Å.

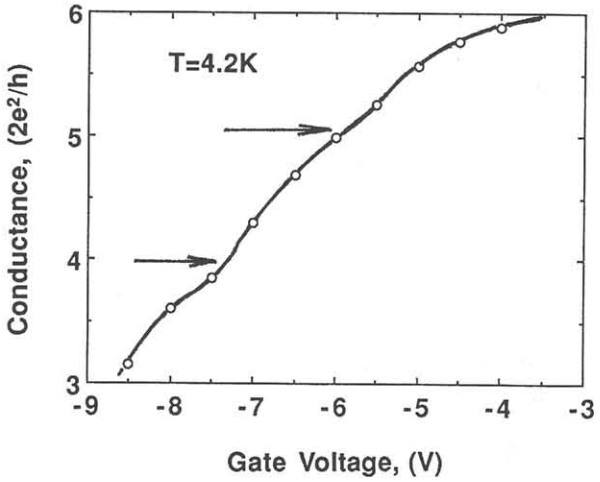

Figure 4.Conductance versus gate voltage of sample C. The nominal width of the wire is 8300Å.

conductance versus gate voltage curves shift upwards with temperature increase, reflecting the Fermi level shift toward higher energy due to thermal ionization of carriers fron the deep donors. Note that the plateaux of various curves coincide to multiples of conductance quantum except the one measured at 114.8K which suffers from drain leakage current problem.

Sample C has a small leakage structure as was the case for sample B. The conductance-gate voltage curve of sample C is shown in Figure 4. Reflecting the wide lateral geometry of 8300Å and narrow sublevel separation, the conductance quantization can be seen just barely at 4.2K.

In summary, quantized conductance was seen only at 4.2K in a 8300Å-wide sample (sample C), but a 3650Å-wide sample (sample B) showed clear quantized conductance and quantized current at temperatures between 58K and 80K. Unfortunately, at 114.8K or above, the sample B showed anomalous quantized conductance presumably due to drain leakage current through buffer layer. A 4600Å-wide device (sample A) showed clear conductance quantization and current quantization at 4.2K. However, it suffered from severe gate lekage problem due to conductive GaSb buffer layer under thin AlGaSb layer. Estimation of sublevel energy separation of these devices will be discussed in conjunction with the quantum-effect-observable temperature in the following section.

4.Discussions

The comparison of simple calculation of sublevel energy separation and temperature of measurements is listed in Table 1. In this calculation, the effective wire widths were used which were calculated by subtracting the width of highly resistive region from the nominal width. The highly resistive region was estimated to be ≈3000Å which is consistent with our previous result[15]. The physical origin of the high resistive layer is not clear at the moment, but we believe that it is related with some form of defects introduced from the surface exposed to atmosphere. We have also niticed that the thickness of the highly resistive layer is thinner (≈1000Å) right after the device fabrication, but soon it widens up and saturates near ≈3000Å range. Finite drain voltage effect[14] and drain-induced-barrier-lowering[15] effect under high bias will also be reported in the conference.

sample	Nominal width, W(Å)	Effective width, Weff (=W-3000Å)	ΔE_{21}	ΔE_{34}	ΔE_{56}
A	4800	1800	2.7meV =8.4kT (at 4.2K)		
B	3650	650		48.3meV =7.32kT (at 77K)	
C	8300	5300		0.723meV =2.27kT (at 4.2K)	1.14meV =3.55kT (at 4.2K)

Table 1. Wire width and estimation of sublevel energy separation of samples A,B andC.

5.Conclusion

We have reported the first demonstration of 1D quantized conductance and quantized currents at 80K in any semiconductor devices. Our results clearly show the potential application of InAs quantum-effect devices which can operate at realistic temperatures. Mesa-etching was shown to be useful method for the lateral confinement of electrons, but at the same time, the presence of highly resistive layer near the exposed surface was infered.

Acknowledgements

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