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Metal/Insulator Heterostructure Quantum Devices on Si Substrate

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Metal/insulator ultrathin heterostructure can be considered as a good candidate for high-speed quantum-effect electron devices. In this paper, we describe the crystal growth and its application to electron devices of metal($CoSi_2$)/insulator(CaF_2) heterostructure which is nearly lattice-matched to sillicon substrate. Resonant tunneling diode operating at room temperature and hot electron transistor with the transfer efficiency over 0.9 at 77K have been demonstrated using this heterostructure system.

1 Introduction

Metal/insulator ultrathin heterostructure can be considered as a good candidate for high-speed electron devices, because high carrier density of the metal and low dielectric constant of the insulator are suitable for the size reduction and high-speed operation of devices[1][2].

In addition, due to very large conduction-band discontinuity at the heterointerface, the interference of electron wave is expected to become large, which may result in high transconductance of quantum-effect devices. In the proposed metal/insulator three-terminal quantum-effect devices, the potential to attain subpicosecond response has been shown theoretically due to these effects[3][4].

We have been studying the epitaxial growth of metal/insulator heterostructure system and its application to quantum-effect high-speed electron devices. As materials for a single-crystalline metal/insulator system, $CoSi_2$ and CaF_2 have been chosen because they have the fluorite lattice structure nearly lattice-matched to Si with the mismatches of -1.2% and $+0.6\%$, respectively.

In this paper, we describe the epitaxial growth of metal($CoSi_2$)/insulator(CaF_2) nanometer-thick heterostructure on Si substrate, fabrication and characteristics of metal/ insulator electron devices, such as resonant tunneling diodes and hot electron transistors.

2 Epitaxial Growth

In order to make $CoSi_2/CaF_2$ epitaxial mulitlayers, we have to find proper epitaxial growth conditions for CaF_2 on $CoSi_2$ and $CoSi_2$ on CaF_2, separately[5][6].

In the case of $CoSi_2$ on CaF_2, the agglomeration of Co on CaF_2 is a critical problem if we use co-deposition of Si and Co with the conventional MBE technique. Thermodynamically, Co atoms tend to minimize the large surface energy at the boundary between the two dissimilar compound materials. This problem was overcome by the following two step growth technique: First, flat 4 monolayers of Si were formed on CaF_2 at the substrate temperature T_s= 500°C using the partially ionized epitaxy with the acceleration voltage V_a= 2kV and ionization current I_e= 350mA. Then, 2 monolayers of Co were deposited on the Si layers by the solid phase epitaxy at temperature <100°C. Since the difference of the surface energy between Co and Si is smaller than that between Co and CaF_2, flat 2 monolayers of $CoSi_2$ were grown on CaF_2 with this technique. $CoSi_2$ layers thicker than 2 monolayers were obtained by repeating this process. The growth rate was determined using the quartz mass sensor in our apparatus.

In the case of CaF_2 on $CoSi_2/CaF_2$, T_s must be lower than about 550°C to avoid thermal deformation and agglomeration of $CoSi_2$ layers. However, the temperature necessary for CaF_2 epitaxial growth is higher than 600°C in conventional MBE technique. We used the partially ionized beam epitaxy to give

external kinetic energy for migration to the evapolated particles. CaF_2 was grown epitaxially on $CoSi_2$ at T_s=450°C with V_a=2kV and I_e=400mA, at which condition the ionization ratio of the CaF_2 beam was about 2%.

Figure 1 shows a cross-sectional TEM lattice image of an as-grown $CaF_2/CoSi_2$ multilayer on Si(111) obtained by the above technique. This image clearly shows epitaxial growth of $CoSi_2/CaF_2$.

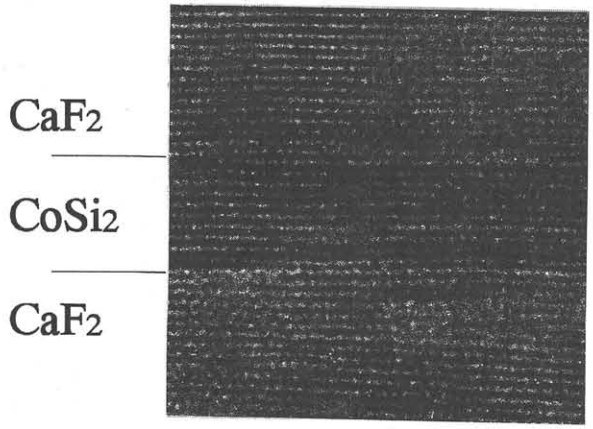

Fig.1 Cross sectional TEM image of a 2.7nm $CoSi_2$ layer sandwiched between CaF_2 layers.

For high-speed electron devices, reduction of the resistivity of thin metal layer is very important. We have found that the resistivity of nanometer-thick $CoSi_2$ layers can be reduced by the *in-situ* thermal anealing after the growth. Resistivity as low as 30 $\mu\Omega$cm, which is comparable to the bulk values, has been obtained for 1.9nm-thick $CoSi_2$ sandwiched between CaF_2 by the anealing at 860°C for 15 minutes[6].

3 Metal/Insulator Electron Devices

3.1 Resonant Tunneling Devices

We fabricated metal/insulator resonant tunneling diode using $CoSi_2/CaF_2$ heterostructure on n-Si(111) mentioned above[8][9]. An example of the device structure and energy-band diagram are shown in Fig.2. The device is composed of triple CaF_2 barriers and double $CoSi_2$ wells with the thickness of a few nanometers. To observe the negative differential resistance in metal/insulator system, the triple barrier structure is necessary instead of the conventional double barrier structure as in semiconductor heterostructures, due to the very large Fermi level[8].

Figure 3 shows examples of the measured current-voltage characteristics of the resonant tunneling diodes. The positive bias stands for that applied to the Si substrate. The negative differential resistance region exists, which indicates the electron wave resonance in the metal/insulator system. The peak-to-valley ratio of the negative differential resistance is typically 2–3

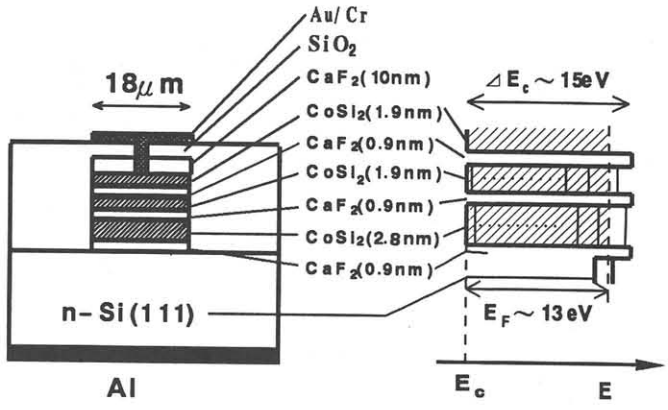

Fig.2 Schematic structure and energy-band diagram of a $CoSi_2/CaF_2$ resonant tunneling diode.

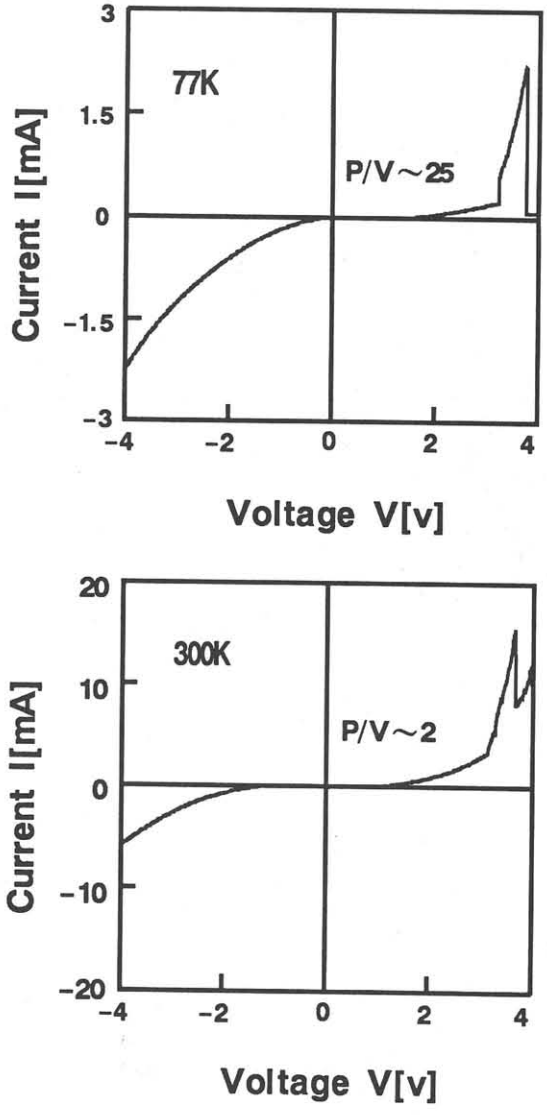

Fig.3 Observed current-voltage characteristics of a $CoSi_2$ /CaF_2 resonant tunneling diode at 77K and 300K.

both at 77K and room temperature, and the largest value was 25 at 77K, as shown in Fig.3. The observed peak-to-valley ratio appears to be reduced by a temperature-dependent leakage current, the origin of which is not clear at present.

The dependence of the voltage at the negative differential resistance on the quantum-well thickness is measured and compared with an approximated calculation with the free-electron and the barrier height of 15eV. It was shown that the measured dependence agrees with the theory by taking into account the uniform deviation of the actual thickness of the metal layers from the design and the fluctuation of the insulator thickness. Double-peaked characteristics was observed for wide quantum wells, in agreement with the theoretical expectation. These results imply that the free-electron approximation is effective in theoretical analysis, although the exact band structure of this system is unknown at present.

A three-terminal quantum-effect device was also fabricated by connecting an electrode to one of the quantum wells in Fig.2 as the base. Transistor action with the negative differential resistance was observed at 77K. The characteristics were similar to the resonant tunneling hot electron transistor (RHET)[10], when the sillicon substrate was used as the collector and the quantum-well layer adjacent to the substrate was used as the base.

3.2 Hot Electron Devices

Metal/insulator hot electron transistor (HET) was also made using $CoSi_2/CaF_2$ on Si(111)[7]. The transistor is composed of a $CoSi_2$(1.9nm) /CaF_2(1.9nm) /$CoSi_2$(1.9nm) tunnel emitter and a CaF_2 (5nm) collector barrier on an n-Si(111) substrate. The emitter-base junction area was $6\times6\mu m^2$.

Transistor action was obtained at 77K in the common-base and common-emitter characteristics. Swift decrease of the base current was observed when the collecter-emitter voltage V_{ce} exceeds the base-emitter voltage V_{be} in the common-emitter characteristics, which shows the transit of electron from emitter to collector through the very thin (1.9nm) metal base layer. The transfer efficiency α ($= I_c/I_e$) over 0.9 (e.g, 0.96 at V_{ce} =5V and V_{be} =3.9V) and the differential gain $\Delta\beta$ ($= \Delta I_c/\Delta I_b$) of $\sim$150 were obtained.

The collector current increased with V_{ce} without saturation, which is different from the semiconductor HETs[11]. Among various possible mechanisms for this result, if the thickness fluctuation is the dominant factor, conventional transistor characteristics can be expected by the improvement of the epitaxial growth as well as the reduction of the device area which experiment is now in progress.

4 Conclusion

Crystal growth of metal($CoSi_2$)/insulator(CaF_2) heterostructure on Si substrate and its application to electron devices were described. Devices utilizing resonant tunneling through metallic quantum wells and hot electron through the insulator conduction band were demonstrated.

We believe that these results are an important step towards realizing novel high-speed quantum-effect devices. Combination of these effects and the investigation of the quantum interference of the electron in the insulator conduction band[4], as well as the size reduction, will enable us to obtain such devices.

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