Extended Abstracts of the 1993 International Conference on Solid State Devices and Materials, Makuhari, 1993, pp. 1029-1031 **D-6-2**

A Surface Emitting Laser with a Common-Anode Configuration for Application to the Photonic Parallel Memory

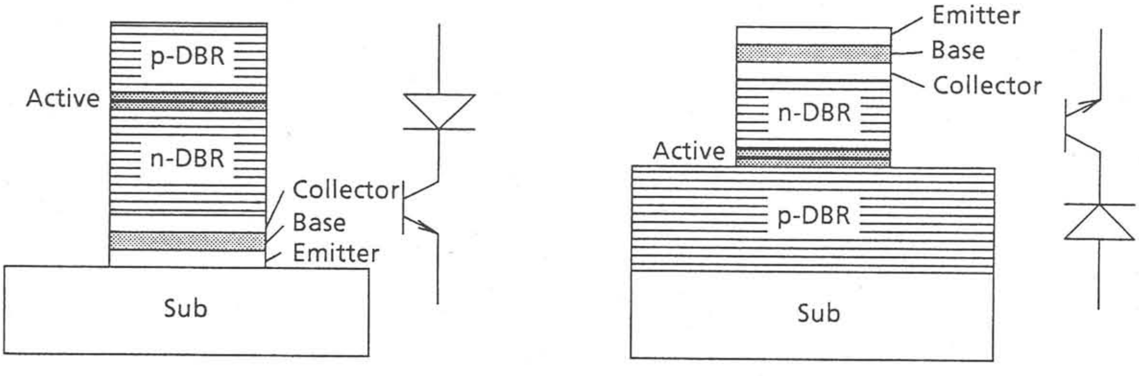
H. Adachi, Y. Kobayashi, T. Chino, and K. Matsuda

Semiconductor Research Center
Matsushita Electric Industrial Co., Ltd.
3-1-1, Yagumo-Nakamachi, Moriguchi, Osaka 570, Japan

We propose a novel configuration of a vertical-cavity surface-emitting laser (VCSEL) and its application to optoelectronic integrated circuits (OEICs). The VCSEL has a p-type bottom mirror on the substrate side. By using a common-anode configuration, lower mesa height and lower electrical resistance can be attained. As the first step to develop the integrated structure, a common-anode VCSEL with a single InGaAs strained quantum well active layer was fabricated. Room temperature pulsed testing was done with 50 ns pulses resulting in a threshold current of 6 mA for the VCSEL with 10-μm diameter. The lasing wavelength was 939 nm.

Vertical-cavity surface-emitting lasers (VCSELs) [1-3] are very attractive because of their surface-normal format, low beam divergence, and good modal properties. One of their promising applications is functional parallel processing. For adding functionality to VCSELs, integrations with other devices have been proposed [4-6]. On the other hand, we have developed a photonic parallel memory (PPM) which is a large-scale two-dimensional array of opto-electronic functional devices [7-9]. The cell of the PPM consists of a light-emitting diode (LED) and a heterojunction phototransistor (HPT). The PPM has bi-stability caused by an optical positive feedback from the LED into the HPT. By substituting the LED to a VCSEL, optical coupling efficiency is expected to be advanced. In this paper, we propose a novel structure suitable for the VCSEL/HPT integration. This configuration can be applied also to optoelectronic integrated circuits (OEICs) including VCSELs and heterojunction bipolar transistors (HBTs).

Connecting an npn-HPT to a VCSEL, the collector must be combined to the cathode of the VCSEL. Using a conventional common-cathode VCSEL, the HPT is arranged under the VCSEL as shown in Fig. 1 (a). This structure is unsuitable for integration because of mesa height. We propose a structure with a common-anode configuration shown in Fig. 1 (b). Using this configuration, it is not necessary to etch all layers of the VCSELs structure. Lower mesa can be obtained by etching the layers just through the active layer.

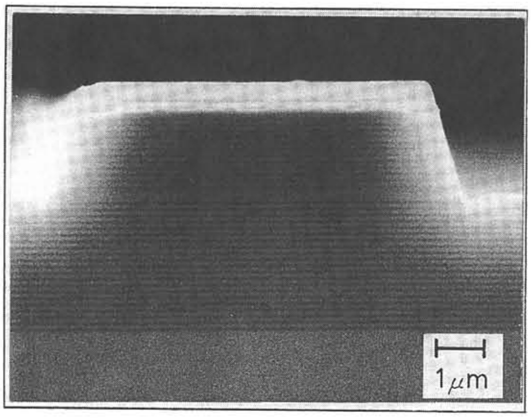


(a) (b)

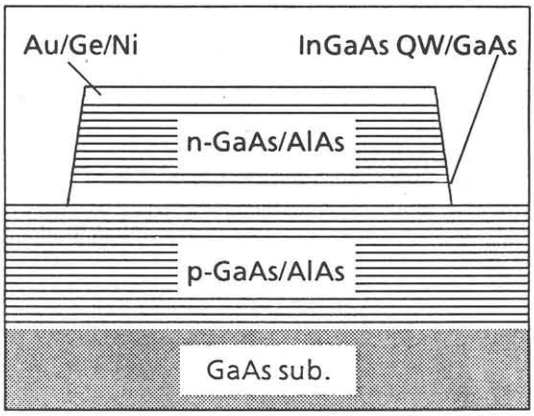
Fig. 1. Schematic cross-sectional view and equivalent circuit of photonic parallel memory with VCSEL. (a) using a conventional common-cathode configuration and (b) using a common-anode configuration.

The proposed structure has another advantage in electrical resistance. High electrical resistance in distributed Bragg reflectors (DBRs) is problem in VCSELs with small diameters. The DBR includes many heterointerfaces with large band discontinuities. A spike at the interfaces prevents current from drifting. Especially in p-type region, the effect is not negligible [10, 11]. In order to solve this problem, several reports introduce graded interface mirrors [12]. However, we propose and utilize the common-anode configuration with abrupt interfaces to realize low resistance more simply. Using the common-anode configuration, the current flows through the p-type DBR with large area. In addition, the third merit is expected in case that HPTs are replaced by HBTs. Since contact metals on the etched surface of base are necessary in HBTs, emitters with smaller size can be attained by using the common-anode structure in comparison with using the common-cathode one.

As the first step to develop the integrated structure, a VCSEL with a common-anode configuration was fabricated. Molecular beam epitaxy was used to grow layers of the VCSEL. The basic layer structure is almost same as conventional VCSEL with InGaAs single quantum well active layer [2]. The mirrors were alternating 1/4-GaAs/AlAs layers with abrupt interfaces. There were 23.5 periods in the bottom mirror and 15 in the top. Be and Si were uniformly doped at 3×10^{18} cm^{-3} in the bottom and the top mirrors, respectively. In order to position the mirrors one wavelength apart, AlGaAs spacer layers were inserted. The growth was capped with a GaAs layer to achieve proper phasing of the reflection from a metal contact on the top of layers. Metal dots composed of Ni on AuGeNi were used as a mask of 10-μm diameter. Reactive ion etching was used to etch just through the active region. A p-contact metal was on

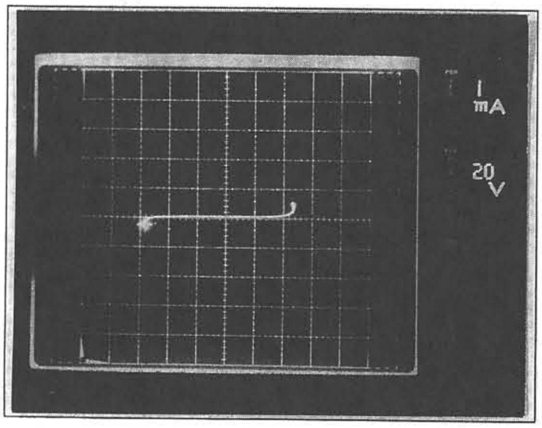


(a)

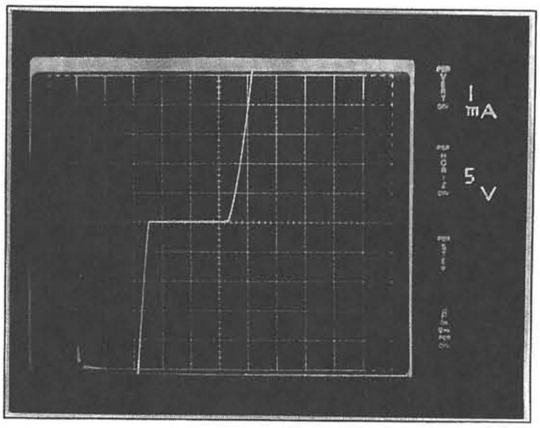


(b)

Fig. 2. (a) SEM micrograph and (b) corresponding schematic cross-sectional view of the VCSEL with a common-anode configuration. The wafer was etched just through the active region by reactive ion etching.



(a)



(b)

Fig. 3. Current vs. voltage characteristics of VCSELs (a) with common-cathode and (b) with common-anode configuration. Contact metals were arranged on the top of the mesa and on the bottom-mirror surface. Horizontal axis are (a) 20 V/div. and (b) 5 V/div., respectively.

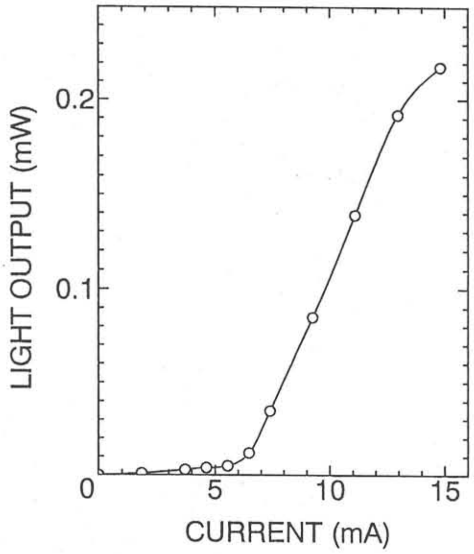


Fig. 4. Pulsed light-output vs. current characteristics in a 10-μm diameter VCSEL at room temperature.

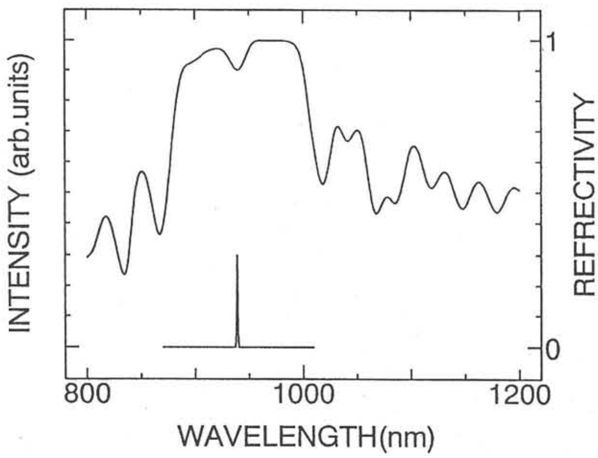


Fig. 5. Reflectivity spectrum of an as-grown laser wafer and the optical output spectrum. Both dip and lasing wavelength are 939 nm.

the exposed bottom-mirror surface. Fig. 2 (a) shows a SEM micrograph of the VCSEL. Etching was stopped just under the active region. Corresponding schematic cross-sectional view is shown in Fig. 2 (b).

Current vs. voltage characteristics are shown in Fig. 3. In case of a common-cathode structure, the turn-on voltage was above 40 V. It is found that the common-anode structure is effective to reduce resistance as shown in Fig. 3 (b). Room-temperature pulsed testing was done with 50 ns pulses resulting in a threshold current of 6 mA and a maximum power of 0.25 mW as shown in Fig. 4. Reflectivity spectrum of an as-grown laser wafer and the optical output spectrum are shown in Fig. 5. Both dip and lasing wavelength are 939 nm. These results indicated that the proposed structure is hopeful technology for large-scale integration.

Acknowledgment

The authors would like to thank Drs. T. Onuma and T. Narusawa for their discussion and continuous encouragement.

References

[1] K. Iga, F. Koyama, and S. Kinoshita, IEEE J. Quantum Electron. 24 (1988) 1845.

[2] J. L. Jewell, J. P. Harbison, A. Scherer, Y. H. Lee, and L. T. Florez, IEEE J. Quantum Electron. 27 (1991) 1332.

[3] R. S. Geels, S. W. Corzine, and L. A. Coldren, IEEE J. Quantum Electron. 27 (1991) 1359.

[4] T. Numai, M. Sugimoto, I. Ogura, H. Kosaka, and K. Kasahara, Appl. Phys. Lett. 58 (1991) 1250.

[5] H. Kosaka, I. Ogura, M. Sugimoto, H. Saito, T. Numai, and K. Kasahara, Jpn. J. Appl. Phys. 32 (1993) 600.

[6] P. Zhou, J. Cheng, C. F. Schaus, S. Z. Sun, C. Hains, K. Zheng, A. Torres, D. R. Myers, and G. A. Vawter, Appl. Phys. Lett. 59 (1991) 2504.

[7] K. Matsuda, H. Adachi, T. Chino, and J. Shibata, IEEE Electron Device Lett. 11 (1990) 442.

[8] H. Adachi, K. Matsuda, T. Chino, and J. Shibata, IEEE Photon. Technol. Lett. 3 (1991) 1013.

[9] T. Chino, K. Matsuda, H. Adachi, and J. Shibata, Electron. Lett. 28 (1992) 641.

[10] G. W. Yoffe, J. Appl. Phys. 70 (1991) 1081.

[11] E. Zeeb, and K. J. Ebeling, J. Appl. Phys. 71 (1992) 5729.

[12] R. S. Geels, S. W. Corzine, J. W. Scott, D. B. Young, and L. A. Coldren, IEEE Photon. Technol. Lett. 2 (1990) 234.