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Bonded Silicon-on-Sapphire Wafers

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Bonded silicon - quartz wafers are ideal for ultra high speed signal propagation due to low value of dielectric constant as presented in Table 1. However, from the view point of heat dissipation, sapphire substrates are superior than that of quartz substrates. The traditional silicon on sapphire wafers, so - called SOS, however, include high density of dislocations ($10^{8\sim10}$ / cm^2). The purpose of this experiment is to obtain dislocation - free silicon layer on sapphire using wafer bonding technique.

1 *Bonding and Thinning Process* A silicon wafer and a sapphire wafer grown by EFG method[1] stick together at room temperature. Long time storage (half year) at room temperature or heating up to 270 C induces voids as shown in Fig. 1 (a) and (b). When silicon wafers with oxide 300 A in thickness are used, void - free bonding occurs. The reason why silicon - quartz wafers[2] without oxide do not induce voids is believed that synthetic quartz glass is amorphous, i. e., from the atomistic point of view, it is bulky and can absorp OH and water on surfaces as to eliminate void formation. On the other hand, sapphire as well as silicon wafers[3] is a single crystal. The void formation of various substrates is drawn schematically in Fig. 2.

Because of the different thermal expansion coefficients between silicon and sapphire as seen in Table 1, thin silicon wafers with 300 μm in thickness are used as suggested by the case of bonded silicon - quartz wafers[2]. However, over 300 C, crack of silicon generates as shown in Fig.1 (c). It seems that a strong bonding between silicon and sapphire wafers instead of hydrogen bonding starts from 300 C. To avoid crack generation, the sticked silicon - sapphire wafers heated up to 270 C are thinned down from 300 μm to 10 μm by grinding. To remove damaged layer induced by diamond abrasive, the silicon layer is etched by KOH solution to 3 μm and then annealed at 450 C, for 2 hrs in dry O2. Finally the silicon layer is thinned down by polishing to ~ 0.5 μm. It is found that if polishing time is long, a part of the silicon layer is wrinkled. Although the large difference of the stock removal rate of silicon between grinding and polishing, i.e., polishing is ~ 0.1 μm / min and grinding is ~ 100 μm / min, the resistance force induced by polishing is greater than that by grinding.

2 *Bonding strength* Figure 3 presents the results of tensile strengthening tests using the samples annealed at 450 C, 700 C and 900 C, for 2 hrs in dry O2. The thicknesses of the silicon layers are separated into three thickness ranges, i.e., < 0.5 μm, 0.5 ~ 1.0 μm and 1.0 ~ 3.0 μm. In the case of the bonded silicon - quartz wafers, there are the critical temperature and the critical thickness for dislocation - and crack - free silicon layers. However, in the case of the bonded silicon - sapphire wafer, within the used temperature and thickness range, these critical values could not be observed. Moreover, although the bonding strengths are high enough, the fracturing of SOI layer which is indicated by the square marked in Fig. 3 occurs with high percentage, which is not observed in other three cases, i.e., silicon - silicon, silicon - oxide and silicon - quartz.

The dislocation and crack generations induced by the difference of thermal expansion coefficients will be confirmed by TEM, x-ray topography and selective etching by the presentation. If dislocation free silicon layers are obtained, although the traditional SOS layers which are epitaxially grown contain the high density of dislocations, the reason why the dislocation - free SOS layers are obtained by the wafer bonding technique will be investigated.

REFERENCES

1) B. Chalmers, J.Cryst. Growth 13 / 14 (1972) 84. 2) T. Abe et al., Jpn. J. Appl. Phys. 32 (1993) 334. 3) T. Abe et al., Jpn. J. Appl. Phys. 29 (1990) L2311.

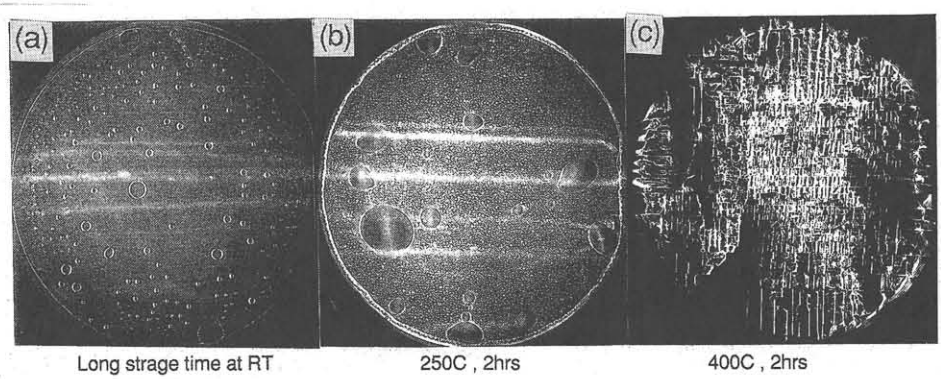

Fig. 1 X - ray topographs of bonded silicon - sapphire wafers (4 inch diameter). Voids generated by long storage time at RT (a), voids generated by anneated by annealing at 250 C without crack. Large voids induced by particls (b), and cracds in silicon at 400 C for 2 hrs in dry O2 (c).

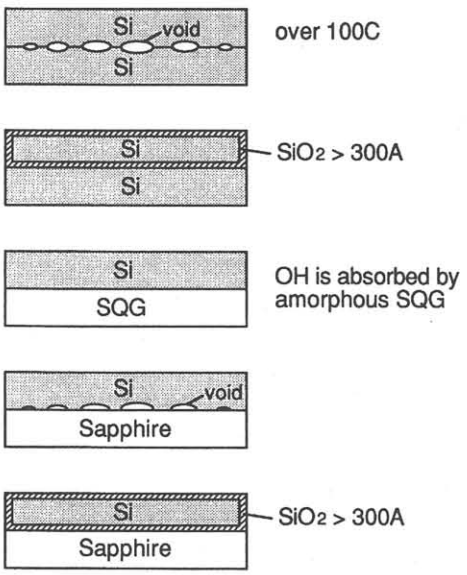

Table 1 Characteristics of various substrates

	Si	Synthetic Quartz Glass	Sapphire
Growth Temp (°C)	Melting Point 1420	Growth Temp >2000	Melting Point 2050
Expansion Coefficient $\times 10^{-6}$/°C (40~400°C)	3.6	0.59	5.0
Dielectric Constant 1MHz , 25 °C	12	3.6	10
Thermal Conductivity W / m·K	125	1.0	42

Fig. 2 The relationship between void formation and oxide layer for various substrates.

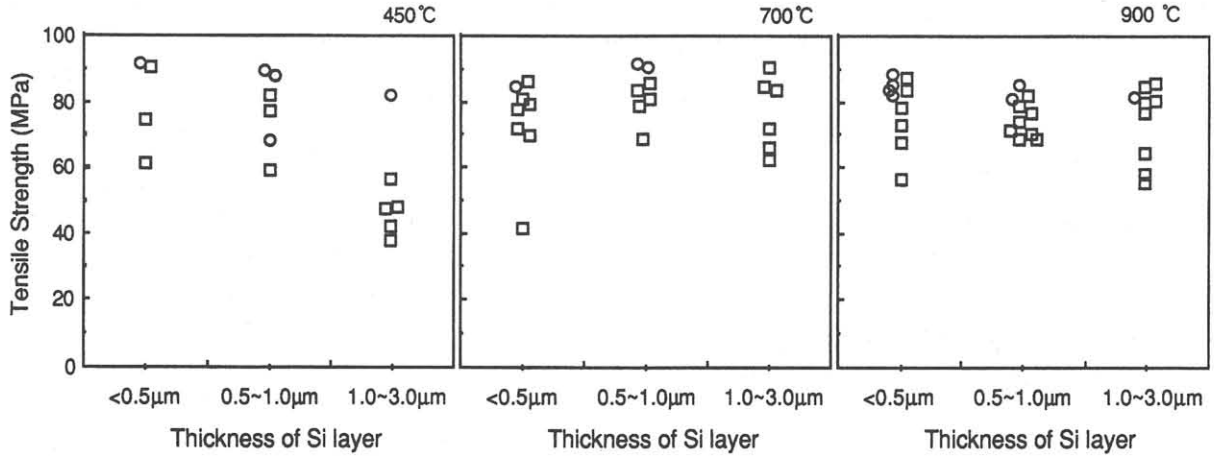

Fig. 3 Thickness dependence of tensile strength of bonded silicon - sapphire samples on varions temperatures.