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Assessment of Hot Carrier Effects on the High Frequency Characteristics of NMOS Transistors

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It is well-known that the degradation of today's advanced (scaled) NMOS transistors due to hot carriers is a serious problem in fabricating reliable devices, and thus extensive researches have been done to study this phenomenon. However, the previous work was mainly focused on the DC analysis, and hot-carrier-induced problems in AC characteristics have not yet been even viewed as important in device reliability. This is, however, not true, particularly for submicrometer NMOSFET aimed at high frequency applications. Therefore, it is highly required to investigate the small signal behavior of the device under the hot carrier stress. In this paper, we report for the first time the hot carrier effects on the AC characteristics of contemporary NMOS transistors, based on 2-D device simulations using MEDICI [1] as well as measurements.

The s-parameters on silicon wafer were measured from the HP8510B Network Analyzer and Cascade microwave probe station. Pad parasitics were eliminated by y-parameter subtraction technique [2]. In order to minimize the measurement error caused by frequent probing, alternate AC measurements and DC bias stressing were performed on the same setup, without lifting the microwave probe tips.

First, we simulated the cutoff frequency (f_T) of fresh NMOS transistors with different channel lengths. For the aging situation, we then injected negative charges in the gate oxide near the drain edge on purpose, keeping the amount of charge in each transistor all the same. The shorter the channel length is, the more degraded f_T is, as expected. Second, we chose a LDD NMOSFET (W/L=50um/1.2um) to measure the magnitude of AC current gain ($|h_{21}|$) as a function of stress time under the Drain Avalanche Hot Carrier (DAHC) and Channel Hot Electron (CHE) conditions. It was found that the degradation by the DAHC condition is worse than that by CHE, which is almost identical to the DC case. Third, we evaluated the degradation of $|h_{21}|$ under the various gate voltages. The result is similar to the above one; the degradation for $V_G<V_D$ (i.e., DAHC condition) is more significant than that for $V_G \cong V_D$ (i.e., CHE condition). It was noteable the maximum AC degradation is observed when the largest substrate currents are detected. Finally we investigated the dependence of hot carrier effects on operation modes of the device. When the device is operated in the current-saturated region, the degradation of $|h_{21}|$ is smaller than that in the linear region, because the pinch-off point is far from the charge-trapped region. This is supported by the fact that when the source and drain terminals are exchanged, the degradation is, regardless of the operation modes, the same since the charge-trapped region is located in the source side in this reverse mode.

In order to assess the significance of the hot carriers in actual circuit performance, we did AC simulations of a comparator composed of 0.8μm NMOS and nominal PMOS devices, assuming that the PMOS devices in the circuit are fresh, and that all the NMOS devices are degraded by the same rate. When the $|h_{21}|$ of the each NMOS transistor is degraded by 8.0%, which is not uncommon under the typical stress condition of contemporary devices, the AC gain and the bandwidth of the circuit are reduced by 12.3% and 1.9% respectively. This implies that the hot carriers could indeed result in the significant degradation of circuit performance in future VLSI technologies.

References

[1]. Technology Modeling Associates Inc., *MEDICI Version1.1 Manual*, 1993.
[2]. A.Fraser et al., "GHz On-silicon wafer probing calibration methods," *IEEE BCTM*, 1988.

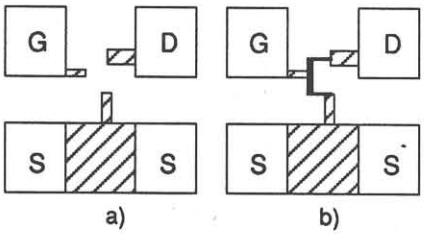

Fig. 1. Test pattern for AC measurements.
a) OPEN Pattern for y-parameter subtraction.
b) DUT Pattern

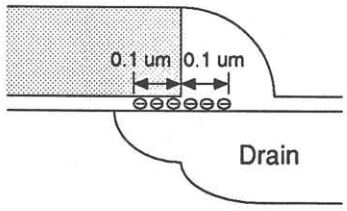

Fig. 2. NMOS structure for device simulations. Gate oxide and oxide spacer thickness are 200Å and 0.17μm respectively.

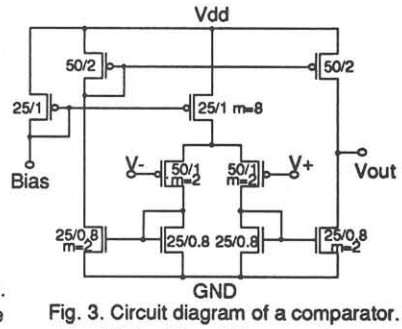

Fig. 3. Circuit diagram of a comparator. The W/L's of transistors are shown. (m is a multiplication factor)

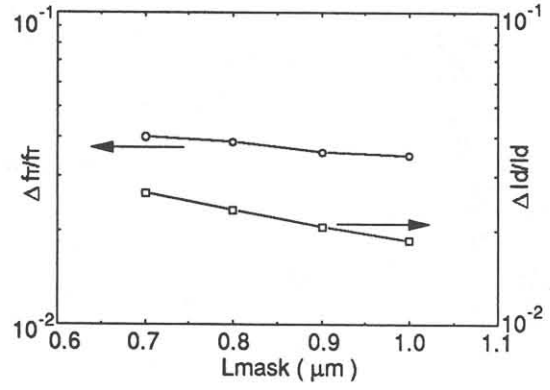

Fig. 4. MEDICI Simulated Δf_T and ΔId when V_D=V_G=3V. The shorter the channel length is, the more degraded f_T is. However, it is not so sensitive as the DC case.

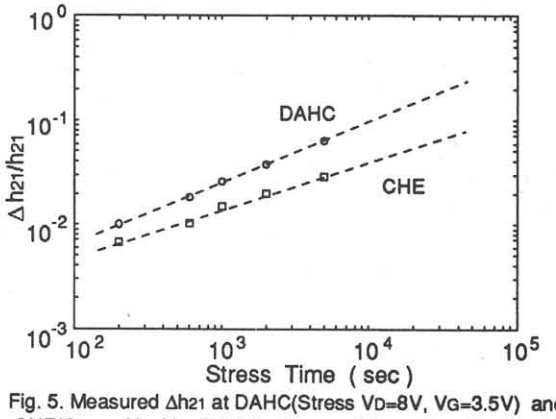

Fig. 5. Measured Δh_{21} at DAHC(Stress V_D=8V, V_G=3.5V) and CHE(Stress V_D=V_G=8V) injection conditions when V_D=V_G=3V. Note that the degradation and its rate (Slope) are worse for DAHC condition.

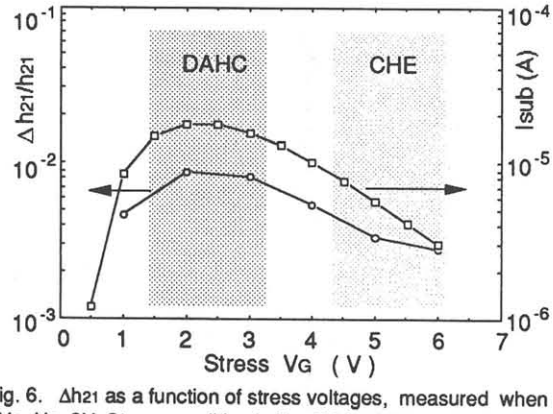

Fig. 6. Δh_{21} as a function of stress voltages, measured when V_D=V_G=3V. Stress condition is V_D=6V for 1000 seconds, with varying V_G. Similar to the results of Fig. 5, the degradation is more significant under DAHC condition. Note that the maximum degradation occurs when the substrate current reaches its peak value.

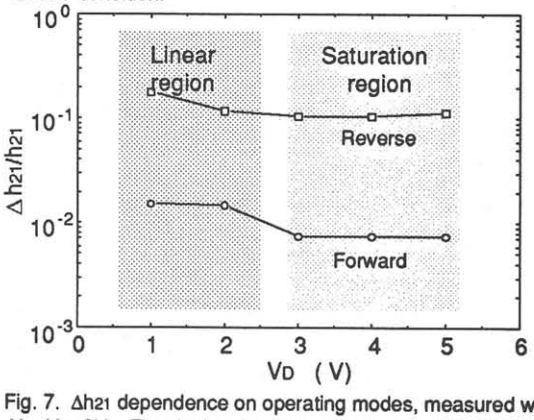

Fig. 7. Δh_{21} dependence on operating modes, measured when V_D=V_G=3V. The device is stressed at V_D=6V, V_G=2V (DAHC condition) for 1000seconds. Under the normal operation (Forward), the degradation in the linear region is larger due to the influence of charge trapped region.When the source and drain terminals are exchanged (Reverse), the degradation is almost the same regardless of operation regions. The severe degradation in the reverse mode results from the asymmetry of source and drain.

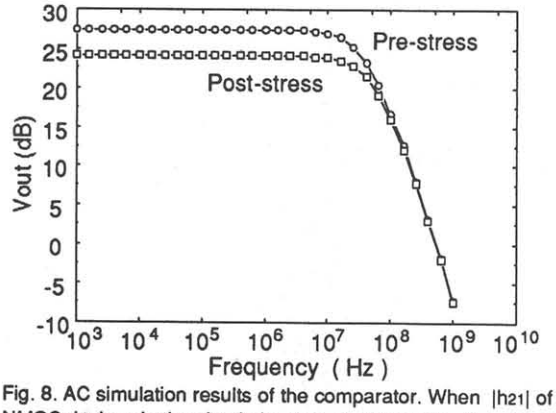

Fig. 8. AC simulation results of the comparator. When $|h_{21}|$ of all NMOS devices in the circuit is degraded by 8.0%, the AC gain and the bandwidth are reduced by 12.3% and 1.9% respectively.

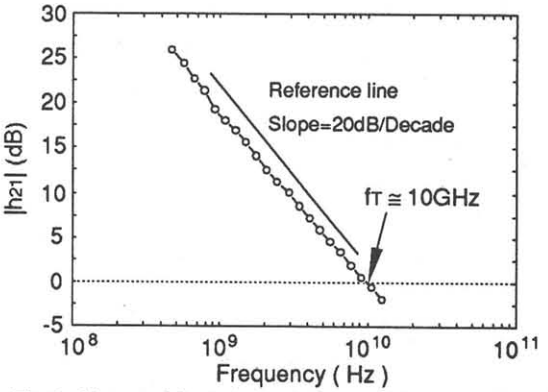

Fig. 9. Measured $|h_{21}|$ of a fresh 1.2um LDD NMOSFET with a 50um gate width.