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Suppression of Interfacial Boron Accumulation and Defect Density in Molecular Beam Epitaxial Silicon

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A low temperature substrate surface cleaning procedure for silicon molecular beam epitaxy(MBE) has been studied. By using HF dipping followed by a two-step annealing, we achieved a great suppression of the interfacial boron spike down to the concentration below $10^{15}cm^{-3}$ and a reduction of the density of deep level defects down to below $10^{12}cm^{-3}$. The preheating temperature to obtain a clear (2×1) reflection high energy electron diffraction(RHEED) pattern can also be lowered to 300°C ~400°C.

1. Introduction

It is well known that the substrate surface treatment is one of the crucial steps in silicon molecular beam epitaxy(MBE). In order to grow high quality epilayer, the substrate surface should be well prepared into a clean, ordered and flat one. The earlier method suggested by Shiraki[1] has been proved to be very successful and thus was adopted in Si MBE for many years. However, it was found later that Shiraki's treatment would result in a boron accumulation at the epilayer-substrate interface[2]. This boron spike at the interface region is believed to be related with the existence of thin oxide layer on the substrate surface[3]. This problem has been solved by using HF etching[3,4], which removes the thin oxide layer and provides a hydrogen-terminated surface on which the boron accumulation will significantly reduce during the epitaxial growth. However, the hydrogen passivation on the surface might not be always complete. There will remain some dangling bonds not saturated and thus may easily combine with the adsorbed carbon atoms. The Si-C bonds once formed are very difficult to break unless the surface is heated to above 1200°C[5]. The carbon contamination especially the Si-C bonds will induce deep level defects in the subsequent growth process. It is therefore obviously important to develop a proper substrate cleaning process that could not only suppress the interfacial boron spike but also prevent the creation of deep level defects during MBE growth. In this work, we illustrate that this could be achieved by adding a low temperature prebake step before final annealing treatment, with the time interval of exposure to air and low vacuum in MBE system as short as possible.

2. Suppression of C-contamination

The improved HF dipping procedure we used is composed by the HF dipping with a two-step annealing procedure.

The samples used were (100) oriented p-type single crystal wafers with the resistivity of 9-12 ohm-cm. After treated by Shiraki's method, the wafer was dipped in a 48%HF:H_2O=1:10 solution for 30 seconds, rinsed by deionized water for 10 seconds, dried in N_2 ambient and then immediately loaded into the introduction chamber of MBE system. The sample was then processed by a two-step annealing treatment, i.e., first, preheating to 300°C for 1 hour in the deposition chamber and second, annealing at 650°C for 10 minutes right before the growth. An unintentionally doped Si epilayer with the thickness of 1.0~1.5mm was grown at the temperature of 600°C and the pressure of 10^{-7}Pa. To perform the C-V and deep level transient

spectroscopy(DLTS) measurements, a Schottky contact was prepared on the top of the epilayer by ex-situ aluminum deposition.

Three different samples have been prepared for comparison. After Shiraki's chemical cleaning, sample A was treated by 900°C annealing in the deposition chamber for 15 min. Sample B and C were treated by HF dipping and immediately loaded into the introduction chamber, maintained there for 5 hours and 30 minutes respectively, then treated by the above two-step annealing in the deposition chamber. The pressure in the introduction chamber was 10^{-5}Pa, where the adsorption of residual gas on surfaces will give different influences for sample B and C.

Figure 1 shows the carrier concentration profile obtained by C-V measurements for these three samples. A carrier concentration spike of $10^{18}/cm^3$ is obviously seen in the interface region of sample A. The secondary ion mass spectroscopy(SIMS) analysis also reveals a boron accumulation peak that coincides with the carrier concentration spike derived from C-V curve. By using HF dipping treatment, the boron spike is greatly suppressed as seen from curve (b) and (c) in Fig. 1. In SIMS measurements, the boron signal was not observed within the detection

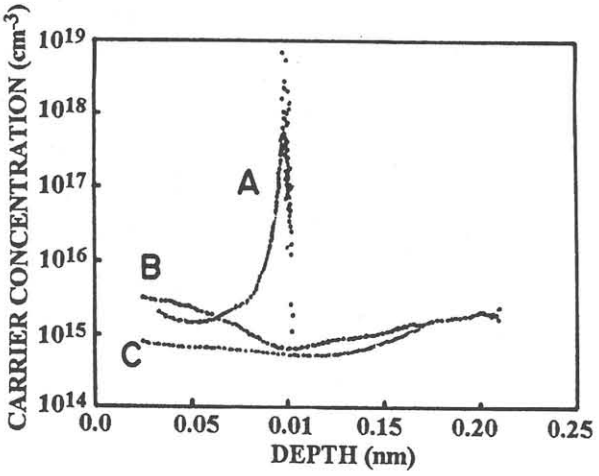

Fig.1 Carrier concentration profile obtained by C-V measurements for three samples

limit. The difference between sample B and C is the existence of a depletion layer at the interface or not. Also the difference is shown in the I-V characteristics of Schottky junctions(Fig.2). The forward I-V curve for sample B behaves as a silicon controlled rectifier(SCR), which implies that there is a thin depletion or inversion layer between the p-type substrate and the unintentionally doped p-type epilayer. The I-V curve of sample C is quite normal.

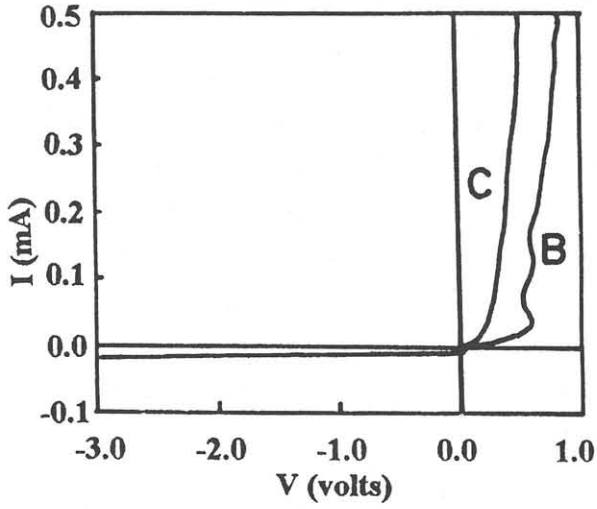

Fig.2 I-V characteristic of Schottky junctions

Another difference between sample B and C are the defect concentration, as shown by the DLTS measurements in Fig.3. For sample C, the concentration of deep level defects is about the DLTS detection limit($10^{12}/cm^3$), while for sample B there exists a signal with the peak position at 220K. The energy level of this defect is derived to be E_c-0.29eV. The defect concentration profile illustrates that this defect is located at the interface. The detail about this defect will be published elsewhere. It is not unreasonable to correlate the carrier depletion in Fig.1(b) with the compensation of shallow acceptors by this defect.

Kanaya et al [5] treated the sample surface with HF dipping and kept it in the load lock chamber(10^{-5}Pa) for 2 hours before heating to 850°C in ultra high vacuum(UHV). Both a boron spike and a depletion layer in the carrier concentration profile were found after MBE growth. Meanwhile, the substrate surface showed a reflection high energy electron diffraction(RHEED) pattern of SiC. To

remove SiC, the substrate has to be heated to 1250°C before MBE growth. As a result, the depletion layer did disappear, but the boron spikes still existed. In their work, an interface free of boron spike and depletion layer could be obtained only if the sample was transferred into UHV(10^{-7}Pa) within the time no longer than 10 minutes after HF dipping.

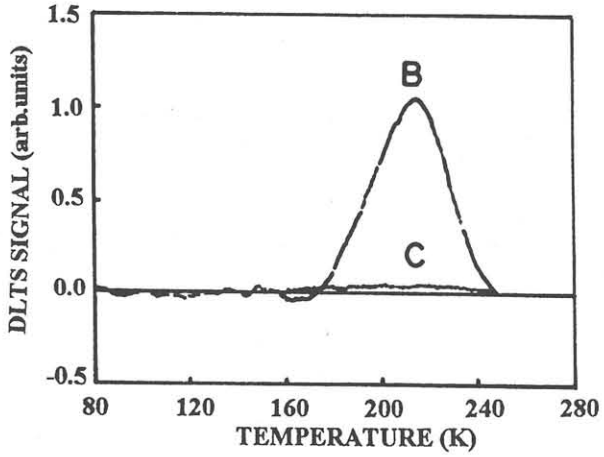

Fig.3 DLTS results for sampleB and C

In our case, no SiC RHEED pattern appears if the substrate is treated by two-step thermal annealing. So that the prebake step is very important. The Auger electron spectroscopy(AES) measurements showed that the C coverage was reduced a factor of 2 by the prebake process in sample B. A further reduction of the C contamination down to below the AES detection limit could be achieved if the total time interval of loading and transferring sample C from air to the growth chamber is no more than 30 minutes. For sample C, a (2×1) RHEED pattern could clearly be seen even after the first step 300°C preheating. In the case of sample B, which was kept in the introduction chamber for 5 hours before annealing, more residual gas molecules will be adsorbed on the surface. A simple preheating at 300°C will not result in a (2×1) RHEED pattern unless the annealing temperature is raised to 600°C. The residual C on the substrate surface is expected to be responsible for the high density of defects at the interface region.

3. conclusion

We present a low temperature substrate surface clean procedure for Si MBE. By using HF dipping followed by a quick load-in process and a two-step thermal annealing, a great suppression of the interfacial boron spike down to the concentration below $10^{15}cm^{-3}$ and a reduction of the concentration of deep level defects down to below $10^{12}cm^{-3}$ have been achieved. As to our knowledge, both of them are the lowest values ever reported in the literature.

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