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Vertical Si-MOSFETs with Channel Lengths Down to 45nm

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Vertical n-MOSFETs with channel lengths down to 45 nm have been grown by Si- molecular beam epitaxy. The growth of thermal oxide on the mesas and the diffusion of the dopants are investigated. We discuss the electrical behaviour of a 50 nm MOSFET.

1) Introduction

The excellent control of layer thickness and doping profile by MBE allows vertical devices on the scale of some ten nanometers. Both subtractive [1] and additive [2] methods have been developed for structuring the epitaxial layers in lateral dimensions down to the submicrometer regime. This is the basis for a reasonable threedimensional integration. The use of vertical devices makes such a threedimensional network even more flexible. The power and elegance of MBE-growth in creating vertical devices is demonstrated by fabricating vertical MOSFETs with channel lengths below the limits of any lateral technology.

2) Experiment

The MBE growth temperature is in general about 500°C for the doped layers. Some of the samples have SPE-grown [3,4,5] contact layers. The instrinsic regions are formed at 700 C. Antimony serves as n-dopant. Boron is used for p-type doping. The growth rate is 1 Å/sec.

We have grown both mesa islands in micro shadow masks [6] and epilayers on (100)-Si substrates. Afterwards the epilayers were structured laterally by plasma etching. At the side walls of the mesas we have fabricated vertical n-channel MOSFETs with source-drain distances varying from 180 nm to 45 nm (fig.1). Some of the samples have a LDD epilayer sequence. The short source-drain distance requires a high channel doping to avoid punch-through. This in turn leads to high electric fields in the pn-junctions. To overcome these problems the channel doping is done in form of a delta doped layer of boron, which is separated from both the source and the drain n^+-region by nominally intrinsic regions of identical thickness.

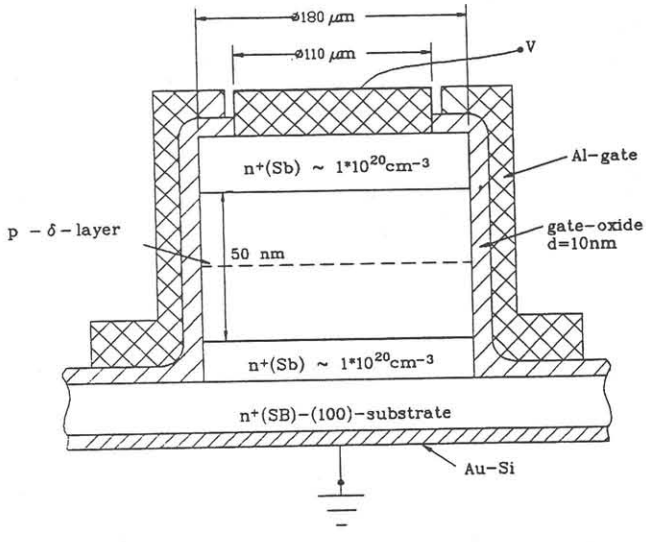

Fig.1: Schematic view of a vertical MOSFET with 50 nm source-drain distance

To retain the sharpness of the doping profiles the oxidation temperature for the gate insulator is limited to 700°C. To improve the break-through behaviour of the gate insulator a 30 nm (resp. 40 nm) CVD-nitride is deposited on top of the oxide. The gate metallization is made of evaporated aluminum. The FET is encapsulated by a sputter oxide. The contact pads consist of sputtered Ti/W and Pt.

3) Results

A sharp and well-defined doping profile is crucial for the function of these extremly short FETs. SIMS profiles prove a good steepness of 6 nm/dek for Sb and 10 nm/dek for B after the complete processing of the FET.

The mesa-grown samples exhibit (111)-surfaces in the channel region (fig.2). (111)-surfaces are energetically preferred by the epitaxial mesa growth[7].

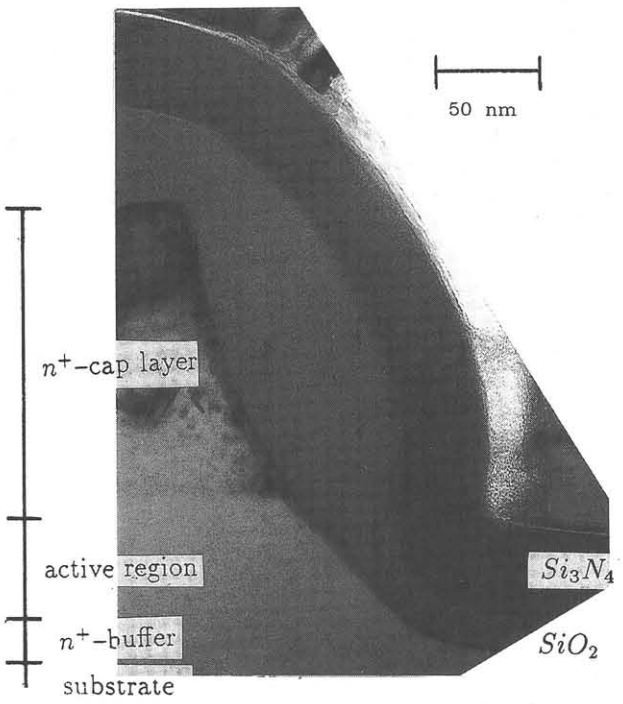

Fig.2: TEM picture (300 000x) of a mesa-grown MOSFET with 50 nm source-drain distance

After oxidation a microroughness of the (111)-surface of less than 3 nm is observed (fig.2). The enhanced growth rate of thermal oxide on highly doped regions allows the growth of a thin (15 nm resp. 25 nm) oxide at the channel region while getting a three to four times thicker oxide at the contacts. This reduces the risk of an oxide break-through at the top edge of the vertical FET. To get an homogenous oxide thickness above the channel we have also grown LDD epilayer sequences with lower doping density ($n=5\ 10^{18}\ cm^{-3}$) in the contact region attached to the channel.

The size of the quadratic mesa structures is 180 µm * 180 µm . So the width of the vertical MOSFET is given by 720 µm and the area of the 'bulk' diode parallel to the FET by $3.24\ 10^4$ μm^2. The room temperature drain and gate characteristics of a 50 nm FET with an effective oxide thickness of 30 nm are shown in fig.3 resp. fig.4.

The measured drain current is the sum of the currents across the transistor and the parallel 'bulk' diode in the interior of the mesa. The current across the diode dominates the drain characteristics at source-drain voltages above 4V. Therefore the saturation regime of the transistor is not observed.

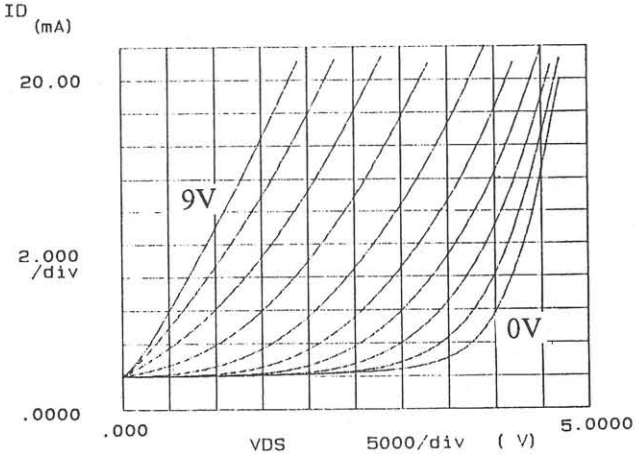

Fig.3: Drain characteristics of a 50 nm MOSFET with 30 nm effective oxide thickness. The gate voltage is varied from 0V to 9V in steps of 1V.

At a source-drain voltage V_{sd} of 1V the leakage current of the transistor is around 30 µA (equivalent to a resistance of 30 kΩ), which means a current density of 1 $nA/\mu m^2$ across the parallel bulk diode. While increasing the gate voltage the drain current saturates at ~ 10 mA for V_{sd}=1V . This means a serial resistance of ~100Ω. The subthreshold swing is determined to be around 1V/dek. The low value of

the subthreshold swing results from the high oxide thickness compared to the source-drain distance and fits well with simulated data.

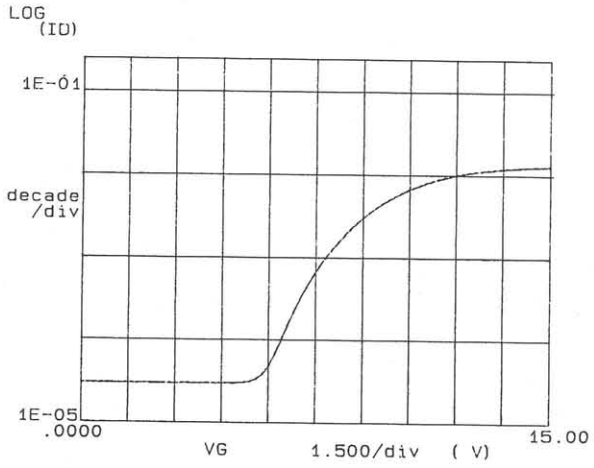

Fig.4: Gate characteristics of a 50 nm MOSFET with 30 nm effective oxide thickness. The drain voltage amounts to 1V.

4) Conclusion

The capability of MBE for the fabrication of ultra short vertical MOSFETs in Si has been demonstrated. The major challenge for processing such devices is an improvement of the low temperature gate oxide. The access to MOSFETs with channel lengths smaller than 50 nm now allows the investigation of ballistic transport or velocity overshoot in silicon.

5) Acknowledgement

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6) References

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