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Growth and Processing of Relaxed $Si_{1-x}Ge_x$/Strained Si Structures for MOS Applications

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Epitaxial growth and processing issues related to strained Si MOSFET fabrication are discussed. The material quality of the graded Ge composition, relaxed $Si_{1-x}Ge_x$ buffer layers is analyzed. The ion implants used to form CMOS "wells" prior to epitaxy are found to degrade the quality of these layers by introducing a high density of misfit dislocation nucleation sites. Rough surface morphology, short misfit dislocation line lengths, and high threading defect densities are correlated with the increased nucleation site density.

Introduction

Strained silicon layers grown on high quality relaxed $Si_{1-x}Ge_x$ buffer layers are of interest for a number of device applications.[1-4] Biaxial tension in the strained Si splits the conduction band degeneracy resulting in higher electron mobility and significant conduction band offset between strained Si and relaxed $Si_{1-x}Ge_x$. We have previously reported enhanced mobility and transconductance in NMOSFETs which employ strained Si channels.[3,4] In this paper, we discuss epitaxial growth and processing issues related to strained Si MOSFET fabrication, in particular the material quality in the device regions.

Device Fabrication Issues

Epitaxial layers are grown by the CVD technique Limited Reaction Processing. Fig. 1(a) illustrates the layer structure suitable for a strained-Si MOSFET. The growth temperatures of the relaxed $Si_{1-x}Ge_x$ and strained Si are 750 and 700°C, respectively. MOSFETs (Fig. 1(b)) were fabricated using a standard process modified for low thermal exposure.[3] The thermal oxidation of the thin (~20 nm) strained Si is a key issue for device fabrication. Both the gate oxide thickness and the strained Si channel thickness are determined by this gate oxidation step. In the present work, we compare the oxidation rate for 15 nm-thick oxides on strained and cubic silicon, at temperatures ranging from 750 to 850°C. To within the 15% measurement uncertainty of Rutherford backscattering (RBS) in a grazing-exit-angle geometry, there is no difference in the observed oxidation rates of strained and CZ silicon.

The lattice mismatch between Si and $Si_{0.7}Ge_{0.3}$ is approximately 1.1%. Strain relaxation during the growth of a thick, constant-composition layer results in the formation of a high density of interfacial misfit dislocations and dislocation segments which thread up to the layer surface. Compositional grading of buffer layers has been shown to dramatically reduce this threading defect density for relaxed $Si_{1-x}Ge_x$ layers grown on Si substrates.[5,6] In this work, relaxed buffer layers are grown at 750°C, with Ge composition graded from 5 to 30% over a thickness of 1.5 μm. Relaxed, constant-composition $Si_{1-x}Ge_x$ layers are grown on top of the graded layer. X-ray diffraction data combined with RBS determination of the Ge fraction show that the strain in this film is 95% relaxed. Cross-section TEM of these structures verifies a high density of dislocations in the graded layer, with a low threading density in the surface layer.

For CMOS process integration, N- and P-type "wells" can be created by high dose implantation and oxidation/drive-in prior to epitaxy. However, residual implant damage in the substrate can dramatically affect the crystal quality of the relaxed $Si_{1-x}Ge_x$ layers. To investigate this effect, several large areas on 4 inch Si wafers were implanted with As and B. The energies and doses for these implants were chosen to yield approximately the same penetration depth (0.25 μm). The time of the oxidation/drive-in was varied to consume different amounts of the original implant-damaged layers. Four different implant conditions and two oxidation cycles were utilized.

Material Analysis

The epitaxial layer structure shown in Fig. 1(a) (without the strained Si layer) was grown on all wafers. Fig. 2 shows Nomarski optical micrographs of the three types of regions on a single wafer after etching in a dilute Schimmel etch. All regions show the characteristic cross-hatch pattern associated with strain field variations. In contrast to the long line length seen in the unimplanted regions, Fig. 2(a), short cross-hatch lines and poor morphology are observed for the relaxed $Si_{1-x}Ge_x$ layers grown over the implanted areas, Fig. 2(b) and (c). These micrographs are representative of the surface morphologies observed for almost all of the implant and oxidation conditions. The one exception is the appearance of layers grown over regions with the highest As dose (10^{15} cm^{-2}). These regions appear similar to the unimplanted areas.

Schimmel etching is not a reliable technique for determining threading defect density in these layers, due to the pronounced cross-hatch pattern. Instead, atomic force microscopy was used on unetched portions of the wafers to determine the threading defect densities. The threading defect density over the B implanted region is very high (~10^7 cm^{-2}) compared to the unimplanted case ($\leq 5x10^5$ cm^{-2}). The threading defect density over the low-dose As implanted region is at least as high as that over the B implanted areas, but is difficult to determine accurately, as defects appear to cluster.

A low density of misfit dislocation nucleation sites has been suggested as a requirement for the growth of relaxed $Si_{1-x}Ge_x$ buffer layers with low threading dislocation densities.[5,6] To compare relative nucleation site densities associated with the various implants, we measured the threading defect density in the underlying Si epitaxial layers. For this purpose, thick Si layers were grown on wafers with As and B implanted regions.

Fig. 3 shows Nomarski micrographs of these Si layers after Schimmel etching. Table 1 lists the measured defect densities and surface morphology of the corresponding relaxed $Si_{1-x}Ge_x$ layers. For all implant conditions which show poor $Si_{1-x}Ge_x$ surface morphology and high threading defect densities, the defect density in the Si layers is high (on the order of 10^7 cm^{-2}). Regions of the wafer which are unimplanted or heavily As implanted display lower Si defect densities and significantly improved $Si_{1-x}Ge_x$ morphology.

Conclusions

Ion implants can be used to introduce damage in a controlled fashion to illustrate the role of nucleation in the growth of relaxed $Si_{1-x}Ge_x$ layers. Rough surface morphology, short misfit dislocation line lengths, and high threading defect densities are correlated with increased nucleation site densities. Minimum threading defect densities are desirable for optimum device performance. However, as shown in Fig. 4, NMOSFETs fabricated in strained Si on B-implanted regions show significantly enhanced mobilities, in spite of high defect densities, compared to devices fabricated in CZ Si control wafers.[3,4]

References

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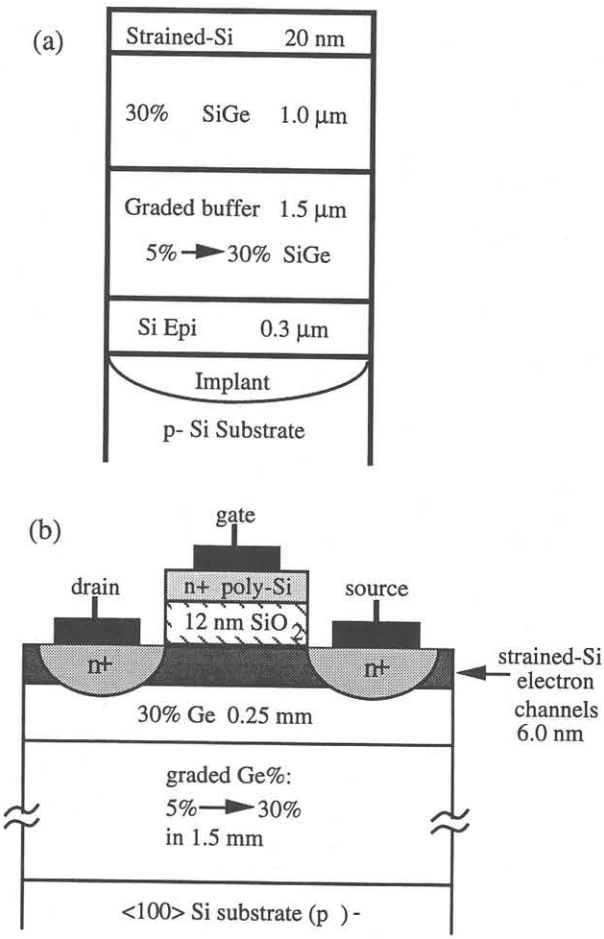

Fig. 1 (a) Epitaxial layer structure used for material analysis; (b) MOSFET device after fabrication from similar epitaxial layers.

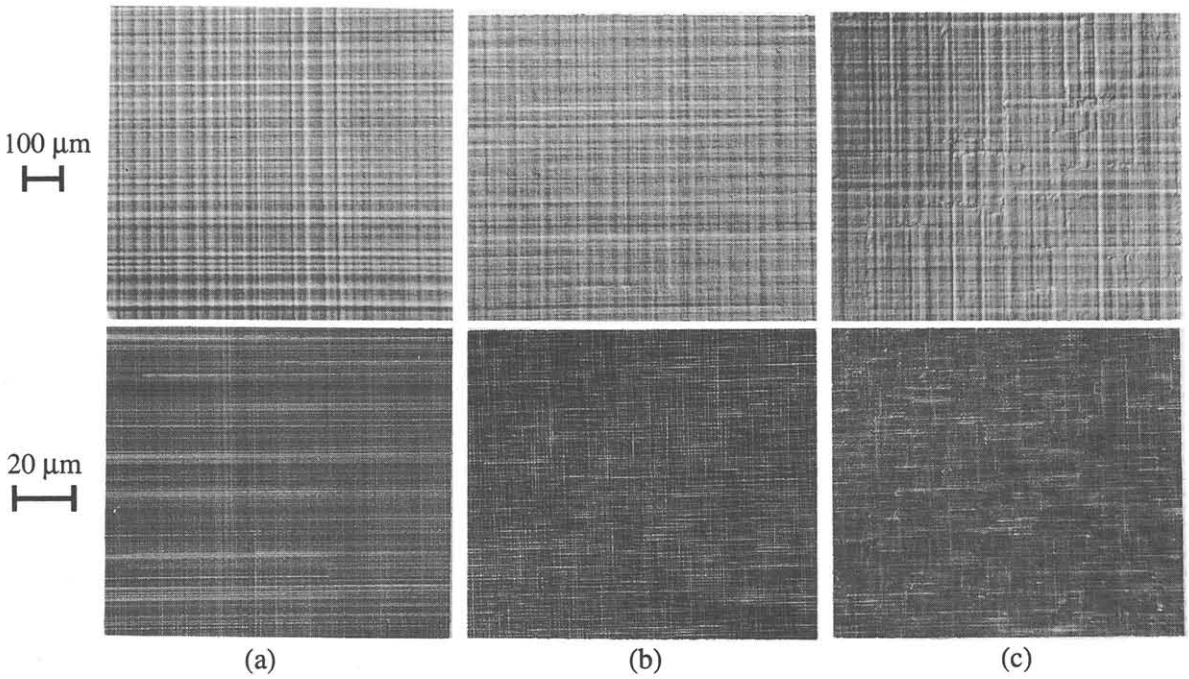

Fig. 2 High and low magnification Nomarski micrographs, after Schimmel etching, of relaxed $Si_{1-x}Ge_x$ layers grown on a single wafer. Before epitaxial growth, regions received (a) no implant, (b) 32 KeV B, $2x10^{15}$ cm^{-2}, and (c) 125 KeV As, $1.4x10^{14}$ cm^{-2}, and a 75 minute drive-in step in wet O_2.

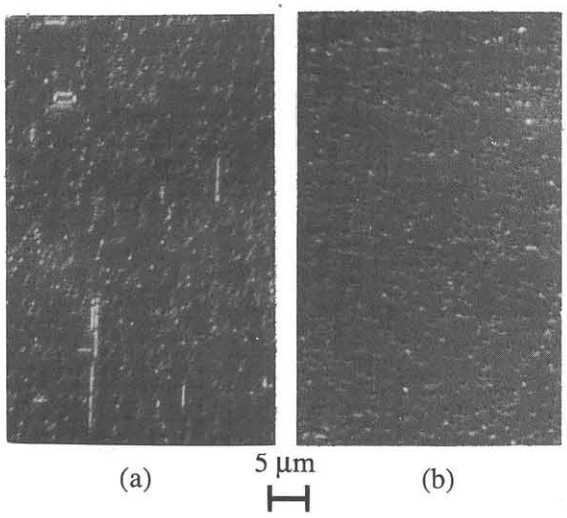

Fig. 3 Nomarski micrographs of Si epitaxial layers after Schimmel etching (a) 125 KeV As, $1.4x10^{14}$ cm^{-2}, (b) 32 KeV B, $2x10^{15}$ cm^{-2}.

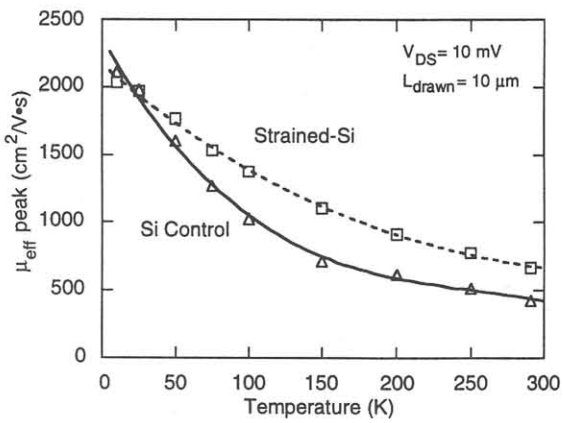

Fig. 4 Peak effective electron mobilities for a strained Si NMOSFET and a CZ Si control over temperature.

Implant Condition	Si Epi Defect Density (cm^{-2})	$Si_{1-x}Ge_x$ Defect Density (cm^{-2})	$Si_{1-x}Ge_x$ Surface Morphology
None	50 - 200	$\leq 5 \times 10^5$	long lines
As 125 Kev 10^{15} cm^{-2}	$1-3 \times 10^5$	–	long lines (similar to above)
B 32 Kev 2×10^{15} cm^{-2}	$1-5 \times 10^7$	$\sim 10^7$	short lines (rough)
As 125 Kev 1.4×10^{14} cm^{-2}	$1-5 \times 10^7$	$\geq 10^7$	short lines (patchy)

Table 1 Summary of Si and $Si_{1-x}Ge_x$ material characterization.