Fully-Selfaligned Al Gate Polysilicon TFT LCD Driver Circuits

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The performance of scanning driver circuits fabricated with low temperature self-aligned Al gate polysilicon TFTs is demonstrated. After the gate electrode patterning, the fabrication process temperature is kept below 400°C to enable the use of aluminum gate electrodes. The low temperature crystallization phenomenon, which occurs when protons are implanted simultaneously with boron or phosphorus dopants, is employed to eliminate the 600°C activation annealing process. A maximum clock frequency of about 2.0MHz is achieved when the driver operating voltage is 24V and the TFT channel length is 12μm.

1. INTRODUCTION

The recent development of a low temperature polysilicon process has been applied to fully scanned active matrix displays. As the size of displays is scaled up, RC time constants along the data and select lines become a significant problem. The availability of an aluminum layer with low sheet resistivity in the low temperature polysilicon process is the key to reducing the RC delay. Formation of the gate electrode of TFTs and the display select lines from the same aluminum layer leads to a reduction in the number of masking processes and an improvement in the display yield. So far, the fabrication of low temperature polysilicon TFTs with chromium or tantalum gate electrodes has been reported.

In this report, the performance of scanning driver circuits fabricated with self-aligned Al gate polysilicon TFTs is demonstrated. Previously we reported a low temperature crystallization phenomenon which occurs when protons are implanted simultaneously with the boron or phosphorus dopant. In this work, the same ion doping technique was used to cause the crystallization phenomenon. The technique is employed to eliminate the (600°C) activation anneal which is usually required in dopant implantation processes.

2. DEVICE FABRICATION

The fabrication process flow is shown in Fig. 1. A SiO₂ buffer layer is deposited on the glass substrate to prevent the TFTs from being contaminated by impurities of the glass. A 100nm amorphous silicon layer is then deposited at 430°C by LPCVD. The amorphous layer is annealed at 600°C for 24 hours in a N₂ atmosphere and then patterned. A 100nm SiO₂ gate oxide layer is then deposited by APCVD at 440°C. The above process sequence is shown in Fig. 1(a) and 1(b). The next step is to form an Al gate electrode. The gate Al layer is deposited at room temperature and patterned. After gate electrode patterning, a phosphorus implant dose of 6×10¹⁵/cm² at an energy of 90keV for n-channel TFTs and a boron implant dose of 6×10¹⁵/cm² at an energy of 33keV for p-channel TFTs are used to form source/drain regions as shown in Fig. 1(c). The ion doping technique is used in the above mentioned implantation process. Protons(1.4×10¹⁶/cm²) are implanted simultaneously with the boron or
After the source/drain region formation, a SiO₂ dielectric layer is deposited on the surface, then contact openings are etched. Finally an Al metallization is deposited and defined as shown in Fig. 1(d).

Figure 1: Fabrication process flow of fully-selfaligned Al gate polysilicon TFT

phosphorus implantation to activate them without annealing.

Figure 2 shows the dependence of the polysilicon film sheet resistance on the phosphorus implant dose. For an implant dose less than $5 \times 10^{14}$/cm² the implanted polysilicon film apparently becomes amorphous and has high sheet resistance. As the dose is increased above $5 \times 10^{14}$/cm², however, the sheet resistance decreases. At a dose of around $2 \times 10^{15}$/cm² the as-implanted sheet resistance is close to that obtained with a 20 hour 600°C anneal. It appears that, at high implant dose, the film is polycrystalline without annealing. An average grain size of 50nm was determined by transmission electron microscopy (TEM)³. The case of a boron implant dose is shown in Fig. 3.

![Graph](image1)

**Fig. 2.** Dependence of polysilicon film sheet resistance upon P⁺ implant dose.

![Graph](image2)

**Fig. 3.** Dependence of polysilicon film sheet resistance upon B⁺ implant dose.
3. TFT CHARACTERISTICS AND PERFORMANCE OF DRIVER CIRCUITS

The transfer characteristics of n- and p-channel TFTs without hydrogenation are listed in Table 1. Channel mobilities are around 46 cm²/Vs for n-channel TFTs and around 27 cm²/Vs for p-channel TFTs.

Figure 4 shows the performance obtained from the above process technology when applied to the CMOS scanning driver circuit illustrated in Fig. 5. The TFT channel length is 12 μm and the total capacitive load is about 15 pF. The maximum clock frequency achieved is about 2.0 MHz at an operating voltage of 24 V.

4. SUMMARY

This paper describes the performance of the CMOS scanning driver circuit fabricated with self-aligned Al gate polysilicon TFTs. The ion doping technique has been employed to enable the use of Al gate electrode.

The performance of polysilicon TFTs is poor in comparison to single-crystal MOSFETs at present. Based on the 2.0 MHz performance obtained in this paper, however, we estimate that 6 μm-gate driver circuits will have a maximum operating frequency of about 8 MHz. Therefore, in the future, as polysilicon TFT performance improves, the above process technique will become increasingly attractive for active-matrix liquid-crystal displays.

<table>
<thead>
<tr>
<th>channel mobility</th>
<th>N-channel</th>
<th>P-channel</th>
</tr>
</thead>
<tbody>
<tr>
<td>mobility</td>
<td>46 cm²/Vs</td>
<td>27 cm²/Vs</td>
</tr>
<tr>
<td>threshold voltage</td>
<td>6.0V</td>
<td>9.7V</td>
</tr>
<tr>
<td>sub-threshold swing</td>
<td>1.5 V/dec</td>
<td>0.7 V/dec</td>
</tr>
</tbody>
</table>

Table 1: TFT characteristics. L=15 μm, W=50 μm, VDS=0.5 V.

REFERENCES