

Poly-Si TFTs with LDD Structure Fabricated at Low Temperature

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Two types of low-temperature poly-Si TFTs with lightly doped drain (LDD) structures have been developed for improving off-current of poly-Si TFTs. The first type has a unique structure in which gate electrodes of poly-Si TFTs are overlapped on LDD regions. The second type has a conventional LDD structure fabricated by combining non mass-separated ion doping technique (I/D) with post-hydrogenation. We confirm sufficiently low off-current (≤ 1 pA) for both poly-Si TFTs.

1. INTRODUCTION

Low-temperature poly-Si TFTs have been investigated for fabricating liquid crystal displays (LCDs) with integrated drivers on glass substrates. When applying the poly-Si TFTs to pixels of LCDs, the high off-current of the poly-Si TFTs has to be reduced. An LDD structure is one way to achieve this.¹⁾ However, low off-current has not been successfully obtained for low-temperature poly-Si TFTs with LDD structures, since crystallinity of poly-Si films in the LDD regions is degraded through an ion implantation process (I/I).

In this paper, we have proposed as solutions two types of low-temperature poly-Si TFTs with LDD structures fabricated through an advanced low-temperature process.

2. EXPERIMENTAL RESULTS

The first type of poly-Si TFTs has a unique structure, as shown in Figure 1. The distinctive feature of this poly-Si TFT is that poly-Si TFT gate electrodes are overlapped on LDD regions. In order to maintain high crystallinity of poly-Si films in the LDD regions and activate impurities implanted by I/I, we utilize fabrication processes as shown in Figure 2. The details of the processes are as follows: At first, 25-nm amorphous silicon

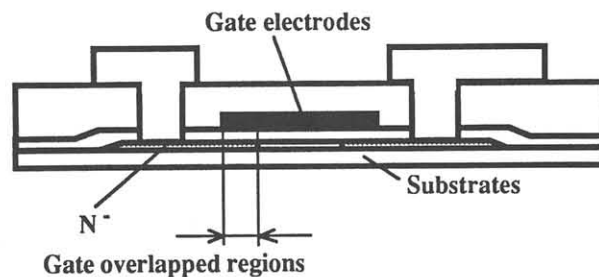


Fig. 1 A cross section of the first type of poly-Si TFTs with LDD structures.

(a-Si) films are deposited on glass substrates by low pressure CVD (LPCVD) at 550°C. Next, channel regions of TFTs are masked with photo-resist and impurities such as phosphorus are implanted by I/I into source and drain regions of TFTs. The photo-resist is then removed and the a-Si films are irradiated by a XeCl excimer laser with energy densities of 243 mJ/cm².²⁾ This process simultaneously activates the impurities and crystallizes the a-Si films. Thus, excellent qualities of poly-Si films in both the channel and the LDD regions are obtained. Finally, 120-nm gate insulators such as SiO₂ are deposited by electron cyclotron resonance CVD (ECR-CVD)³⁾ and gate electrodes such as Cr are formed on top of the gate

insulators. Figure 3 shows electrical characteristics of the first type of poly-Si TFTs. Despite a structure whose gate electrodes are overlapped on the LDD regions, the poly-Si TFTs have a sufficiently low off-current (≤ 1 pA) with a dose of $5 \times 10^{13} \text{ cm}^{-2}$.

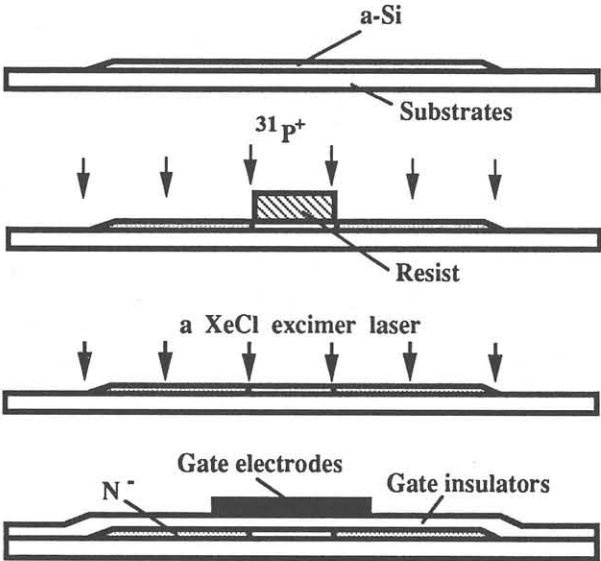


Fig. 2 Key processes for fabricating the first type of the poly-Si TFTs with LDD structures.

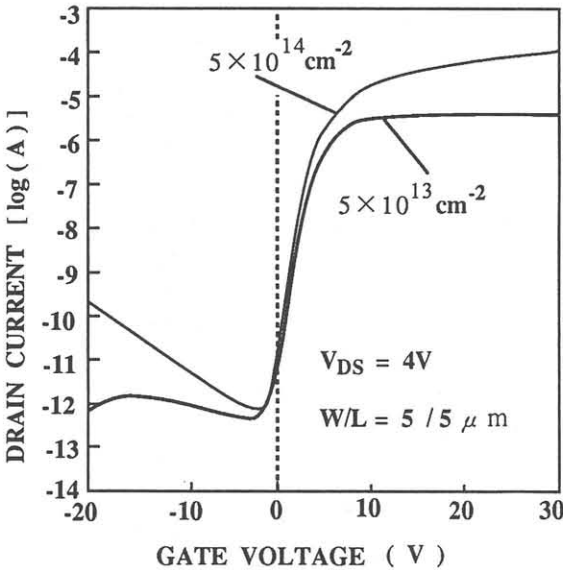


Fig. 3 Electrical characteristics of the first type of poly-Si TFTs depends on the dose of N⁻ regions.

The second type of poly-Si TFTs has a conventional LDD structure fabricated by I/D. The details of I/D were described elsewhere.⁴⁾ When using I/D, it is noted that crystallinity of poly-Si films is maintained despite a high dose of impurities and that the impurities implanted by I/D are activated through 300°C furnace annealing.⁵⁾ Thus, a conventional LDD structure with high crystallinity of poly-Si films can be realized by using I/D. However, it has been difficult to activate a small dose (below $1 \times 10^{14} \text{ cm}^{-2}$) of impurities such as phosphorus implanted by I/D through 300°C furnace annealing. In order to solve this problem, we have developed a new fabrication process featuring I/D. Figure 4 shows a schematic diagram of the new fabrication process. We use 50-nm poly-Si films crystallized by a XeCl excimer laser for channel layers of poly-Si TFTs. A small dose of phosphorus atoms is implanted into LDD regions of poly-Si TFTs through 120-nm SiO₂ by I/D. The doping conditions are as follows: 5% PH₃ diluted with H₂ is used for a doping gas, and the accelerating voltage is 80 keV. Hydrogen atoms are also implanted into the LDD regions by I/D with the accelerating voltage of 20 keV, a dose of $3 \times 10^{15} \text{ cm}^{-2}$, and a doping gas of 100% H₂. Hydrogen atoms can terminate defects of the LDD regions without any degradation in the channel layers by this method. Figure 5 shows the dependence of the sheet resistance of 50-nm poly-Si films (in which impurities are implanted by these processes) on the dose of phosphorus ions.

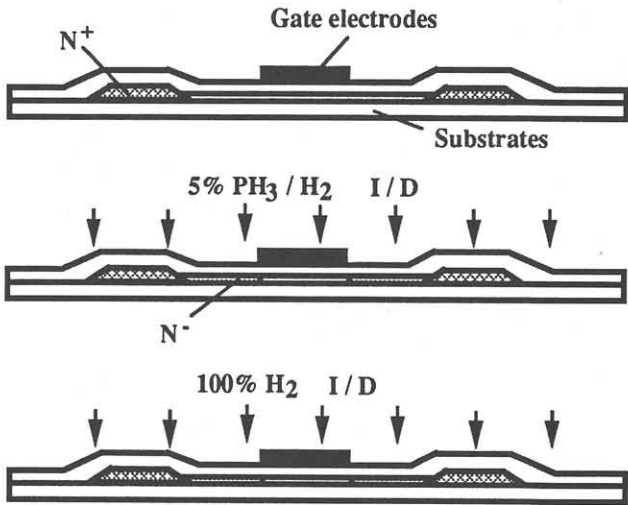


Fig. 4 A schematic diagram of the new fabrication process featuring I/D.

Activation annealing is carried out for 60 min in N₂ at 300°C. A small dose of phosphorus atoms is satisfactorily activated with 300°C furnace annealing. Figure 6 shows the drain current (I_D)-gate voltage (V_G) characteristics of the second type of poly-Si TFTs with LDD structures. Off-current falls below a dose of 3×10^{13} cm⁻².

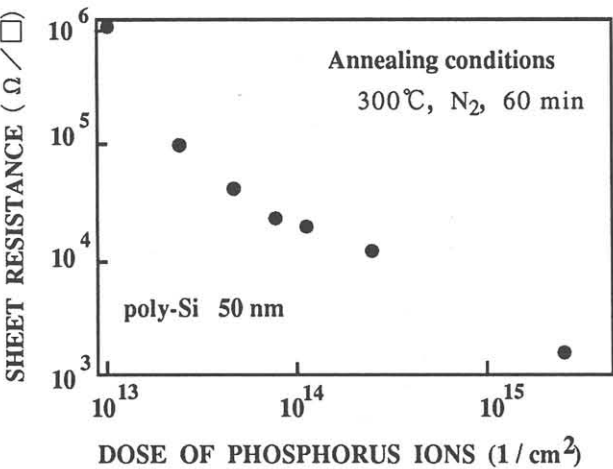


Fig. 5 The dependence of the sheet resistance of 50-nm-doped poly-Si films on the dose of phosphorus ions.

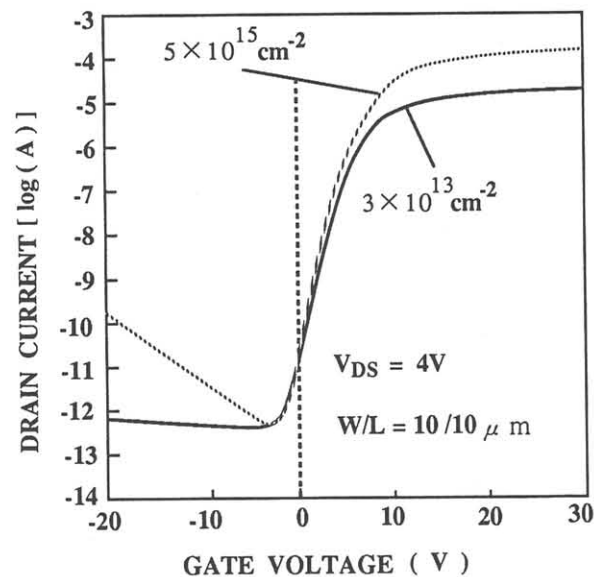


Fig. 6 I_D - V_G characteristics of the second type of poly-Si TFTs with LDD structures. For comparison, the characteristics of conventional poly-Si TFTs are also indicated by a broken line.

3. CONCLUSION

In conclusion, two types of low-temperature poly-Si TFTs with LDD structures have been developed. Whether the gate electrodes are overlapped on the LDD regions or not, off-current has been reduced. The reasons are that a low trap density of poly-Si films in LDD regions are achieved through the process mentioned above. When employing these technologies, single-gate poly-Si TFTs can easily be applied to LCD pixels. They hold promise for use in high resolution and high pixel density LCDs with integrated drivers fabricated on glass substrates.

4. REFERENCES

- 1) M. Yazaki et al.: Jpn. J. Appl. Phys. **31**(1992) 206.
- 2) T. Hashizume et al.: Extend Abstract of the Conference on Solid State Devices and Materials, 638(1991).
- 3) H. Ohshima and S. Morozumi: International Electron Devices Meeting Technical Digest, 157(1989).
- 4) S. Inoue et al.: International Electron Devices Meeting Technical Digest, 555(1991).
- 5) M. Matsuo et al.: Jpn. J. Appl. Phys. **31**(1992) 4567.