Extended Abstracts of the 1993 International Conference on Solid State Devices and Materials, Makuhari, 1993, pp. 443-445

Structural Dimension Effects of Plasma Hydrogenation on Low-Temperature Poly-Si TFT's

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The effects of hydrogen passivation on various dimensional N- and P-channel polycrystalline silicon (poly-Si) thin-film transistors (TFT's) fabricated using a maximum temperature of 600 ^oC were analyzed systematically. As the channel length of poly-Si TFT's was decreased from 20 μm to 2.5 μm, device characteristics were improved significantly with hydrogenation time. However, hydrogenation effects on the characteristics of TFT's, of which channel width was varied from 2.5 μm to 20 μm, was almost identical. In thin active layer (50 *nm*) TFT's, the device performance was improved significantly compared with thick (100 *nm* and 150 *nm*) devices with hydrogenation time but the gate poly-Si thickness may not be directly related with hydrogenation process. Our experimental results may support the model that the hydrogen atoms diffuse along channel region while the diffusion of hydrogen atoms through gate poly-Si is negligible.

1. INTRODUCTION

Low temperature (< 600 ^oC) polycrystalline silicon (poly-Si) thin film transistors (TFT's) may be the promising device for large area display systems due to their large mobility. However, it is well known that grain boundaries exert a profound influence on the device characteristics and degrade carrier transport. The hydrogen passivation of grain boundaries may be a key process to improve the performance of poly-Si TFT's.

Various possible pathways proposed for introduction of hydrogen into the poly-Si TFT channel region include diffusion through poly-Si gates and gate oxides or through the quartz substrate and active poly-Si layer into the channel region[1] and hydrogen diffusion in polycrystalline silicon thin film is analyzed[2]. The purpose of our work is to identify a dominant hydrogen path in poly-Si TFT's. It has scarcely reported that how the hydrogenation effects on poly-Si TFT's with various device geometry. We have investigated the hydrogenation effects on the poly-Si TFT's with various active layer thickness (50, 100 and 150 *nm*), gate poly-Si thickness (100 and 250 *nm*) and channel dimensions (W = 2.5 μm ~ 20 μm, L = 2.5 μm ~ 20 μm).

2. EXPERIMENTAL

The amorphous silicon (a-Si) for active layer, of which thickness varied from 50 *nm* to 150 *nm*, was deposited by LPCVD on oxidized silicon wafers at 560 ^oC. These a-Si films were crystallized by thermal annealing at 600 ^oC for 48 *hrs* in N_2 ambient. After definition of silicon islands, 100 *nm* thick silicon dioxide film deposited by APCVD was used as a gate dielectric layer. The thickness of poly-Si gate, which was deposited in the amorphous phase by LPCVD at 560 ^oC and crystallized by thermal annealing at 600 ^oC, varied from 100 *nm* to 250 *nm*. The polysilicon for gate and source/drain electrodes were heavily doped by self-aligned P^+ and BF_2^+ implatation at an energy of 30 *keV* and dose of 5×10^{15} cm^{-2}. N- and P-channel polysilicon TFT's were fabricated simultaneously using a maximum temperature of 600 ^oC. Plasma hydrogenation was performed in a plasma reactor with various time. The hydrogen plasma treatment conditions were 300 ^oC and 1 *Torr* in hydrogen. The rf power density was 0.07 W/cm^2 at 13.56 *MHz*. The device characteristics, such as field effect mobility (μ_{fet}) and threshold voltage (V_{th}), were measured as a function of hydrogenation time. The trap state density (N_t) of poly-Si layer was extracted by the linearity of $\ln(I_d/V_g)$ vs. $1/V_g$ curve[3].

3. RESULTS AND DISCUSSION

The variation of threshold voltage with different hydrogenation time as functions of channel length and width for N- and P-channel poly-Si TFT's are shown in Figs. 1 and 2. As the channel length of poly-Si TFT's, where the channel width was fixed at 20 μm, was decreased from 20 μm to 2.5 μm, threshold voltage reduced significantly with hydrogenation time as shown in Fig. 1. The effects of hydrogen passivation on short channel device is relatively significant compared with those on long channel device. However, hydrogenation

effects on the characteristics of TFT's, of which channel width was varied from 2.5 μm to 20 μm while channel length was fixed at 20 μm, was almost identical as can be seen in Fig. 2. The channel width does not influence on the hydrogenation effects while the channel length plays a key role for hydrogenation effects on the device performance.

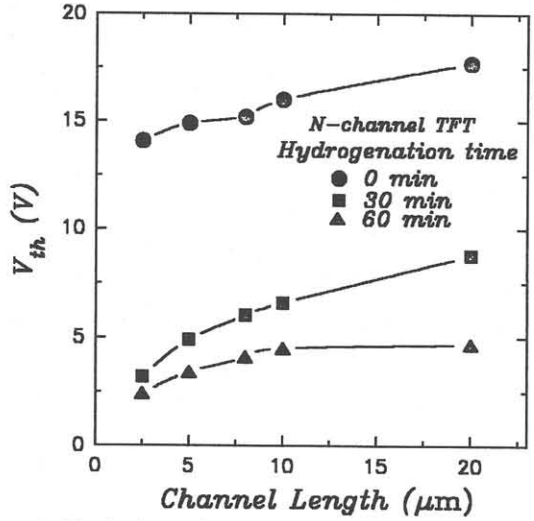

Fig. 1. Variation of threshold voltage as a function of channel length for W = 20 μm N- and P-channel poly-Si TFT's with different hydrogenation time. The thickness of gate and active poly-Si is 100 *nm*.

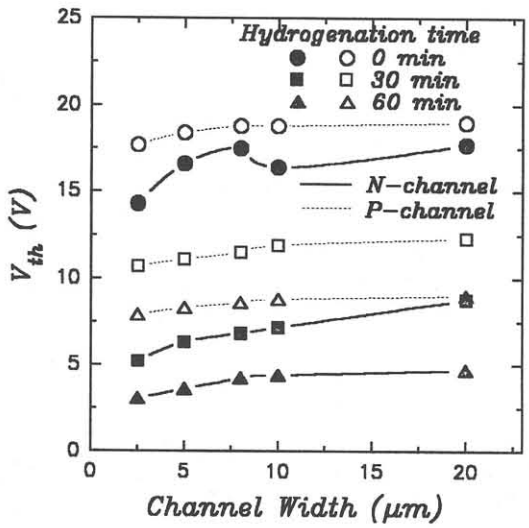

Fig. 2. Variation of threshold voltage as a function of channel width for L = 20 μm N- and P-channel poly-Si TFT's with different hydrogenation time. The thickness of gate and active poly-Si is 100 *nm*.

It was also observed that the hydrogenation effects depend on active poly-Si layer thickness. Fig. 3 shows threshold voltage shift and normalized increment of field effect mobility as a function of hydrogenation time for various active poly-Si thickness. Gate poly-Si thickness of N-channel poly-Si TFT's was 100 *nm* and channel length and width were 20 μm and 10 μm, respectively. In thin active layer (50 *nm*) TFT's, the device performance was improved significantly compared with thick (100 *nm* and 150 *nm*) devices with hydrogenation time. Fig. 4 shows the normalized reduction of trap state density with hydrogenation time for different active poly-Si thickness. The trap state density of poly-Si layer before hydrogenation is about 4~5 $\times 10^{12}$ $/cm^2$ and that after hydrogenation is about 2~3 $\times 10^{12}$ $/cm^2$. It can be seen that the reduction of trap state density in 50 *nm* active poly-Si TFT's is much larger than that in thick devices.

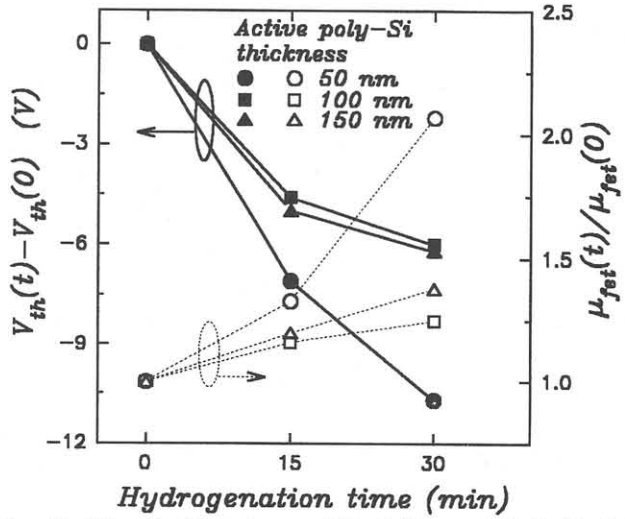

Fig. 3. Threshold voltage shift (ΔV_{th} = V_{th}(t)-V_{th}(0)) and normalized increment of field effect mobility (μ_{fet}(t)/μ_{fet}(0)) as a function of hydrogenation time for various active poly-Si thickness. Gate poly-Si thickness of N-channel poly-Si TFT's was 100 *nm* and W/L = 20/10 $\mu m/\mu m$. The symbol *t* refers to hydrogenation time.

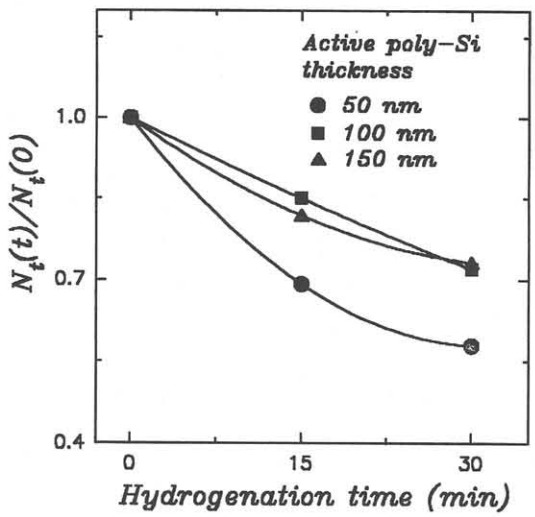

Fig. 4. Normalized variation of trap state density with hydrogenation time for various active poly-Si thickness (50, 100 and 150 *nm*). The symbol *t* refers to hydrogenation time.

Hydrogenation effects of poly-Si TFT's with different gate poly-Si thickness are examined as a function of hydrogenation time. Threshold voltage (V_{th})

as a function of hydrogenation time for N-channel poly-Si TFT's with different gate poly-Si thickness and various channel dimensions is represented in Fig. 5. Hydrogenation effects of poly-Si TFT's with 100 *nm* and 250 *nm* gate poly-Si thickness are almost identical in three different channel dimensions. For short channel devices (W/L = 20/5 $\mu m/\mu m$), the field effect

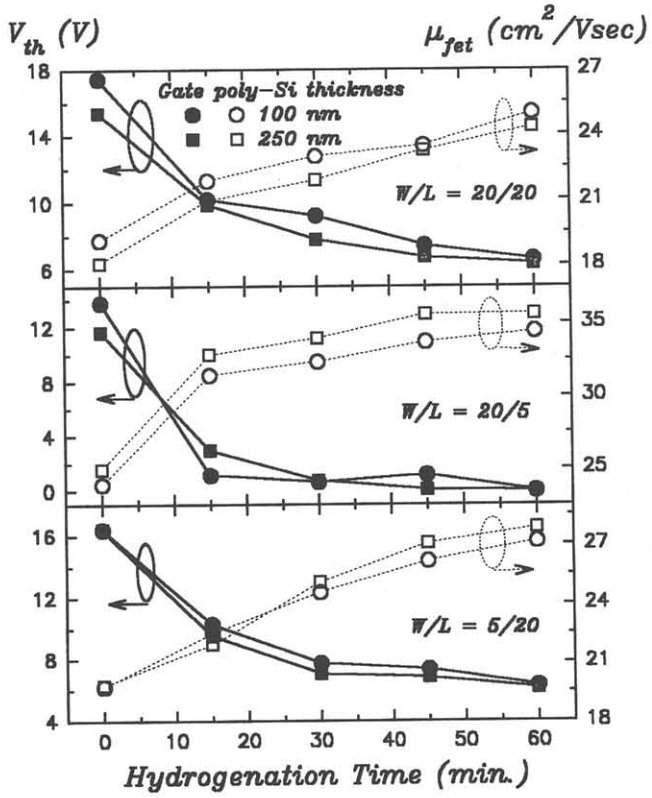

Fig. 5. Threshold voltage (V_{th}) and field effect mobility (μ_{fet}) as a function of hydrogenation time for N-channel poly-Si TFT's with different gate poly-Si thickness and various channel dimensions.

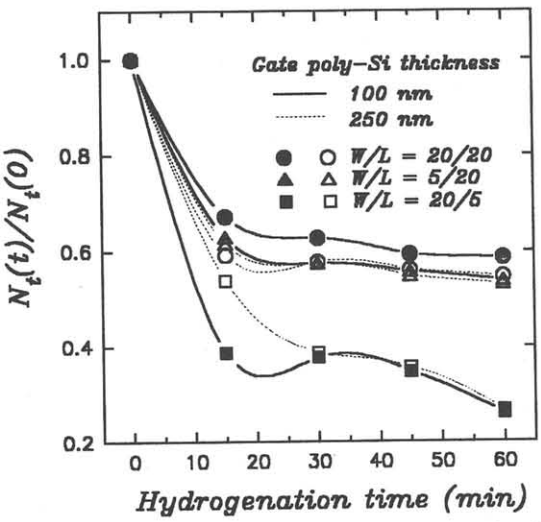

Fig. 6. Normalized variation of trap state density with hydrogenation time for different gate poly-Si thickness and various channel dimensions. The symbol *t* refers to hydrogenation time.

mobility was increased and the threshold voltage was decreased significantly in a short hydrogenation time. On the contrary, the field effect mobility and the threshold voltage of long channel devices (W/L = 20/20 and 5/20 $\mu m/\mu m$) were slowly varied with hydrogenation time. Fig. 6 shows the normalized variation of trap state density with hydrogenation time for various channel dimensions. The trap state density of poly-Si TFT's before hydrogenation is about 4~5 $\times$ 10^{12} $/cm^2$. After hydrogenation, the trap state density is about 2 $\times$ 10^{12} $/cm^2$ for W/L = 20/20 and 5/20 $\mu m/\mu m$ TFT's and about 1 $\times$ 10^{12} $/cm^2$ for W/L = 20/5 $\mu m/\mu m$ devices. The reduction ratio of trap state density is almost identical with the same channel dimensions irrelevant with gate poly-Si thickness probably due to the facts that the diffusion of hydrogen atoms through gate poly-Si may be negligible.

4. CONCLUSION

The effects of hydrogen passivation on various dimensional low-temperature poly-Si TFT's were analyzed systematically. As the channel length of poly-Si TFT's, where the channel width was fixed at 20 μm, was decreased from 20 μm to 2.5 μm, threshold voltage reduced significantly with hydrogenation time. But, hydrogenation effects on the characteristics of TFT's, of which channel width was varied from 2.5 μm to 20 μm while channel length was fixed at 20 μm, was almost identical. In thin active layer (50 *nm*) TFT's, the device performance was improved significantly compared with thick (100 *nm* and 150 *nm*) samples with hydrogenation time. Hydrogenation effects of poly-Si TFT's with 100 *nm* and 250 *nm* gate poly-Si thickness are almost identical in three different channel dimensions.

In summary, active layer thickness and channel length play an important role to control the hydrogenation effects on the device performance while the variation of gate poly-Si thickness and channel width do not control. This behavior is believed to be due to the fact that the hydrogen atoms may diffuses along channel region while the diffusion of hydrogen atoms through gate poly-Si may be negligible.

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