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A Study of Short Channel Behavior of Accumulation Type SOI MOSFETs

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This paper presents a theoretical analysis of the short channel behavior of accumulation mode (AM) SOI MOSFETs with gate lengths shrinking into the 0.1μm region. A two-dimensional analytical model developed by the authors for inversion mode (IM) SOI MOSFETs[1] is modified for AM devices. The results are supported by numerical device simulation. An inherently higher sensitivity of the AM SOI MOSFET to variations of channel doping, SOI thickness and substrate voltage is found compared with the IM transistor. The key factor for controling short channel effects in the AM SOI MOSFET is the thickness of the SOI layer.

INTRODUCTION

Fully depleted accumulation mode (AM) MOS transistors are unique devices only obtainable on SOI. They have received considerable attention for developing high performance CMOS applications on thin SOI films[2]. AM SOI MOSFETs show high current drivability and attenuated short channel and hot carrier effects. Useful threshold voltages are achievable by using a reverse gate type device design with lightly doped channel. On the other hand they are known to suffer from punchthrough and leakage problems at the back channel/buried oxide interface in short channel devices[3]. In this paper the short channel behavior of AM SOI MOSFETs is investigated for applications towards the sub-quarter micron regime down to 0.1μm gate length. For this purpose a two-dimensional analytical model has been developed which is supported by numerical device simulation.

ANALYTICAL MODEL

In order to solve the two-dimensional Poisson equation in the subthreshold region a parabolic vertical potential distribution inside the SOI layer is assumed. Expressions for the minimum front and back surface potentials can be derived which in turn are used to calculate the subthreshold slope as well as the threshold voltage both for IM and AM SOI MOSFETs. The subthreshold current conduction mechanism is determined from the potential distribution in the SOI film and the appropiate formula can be chosen. The investigated device structure is depicted in Fig. 1. An n-

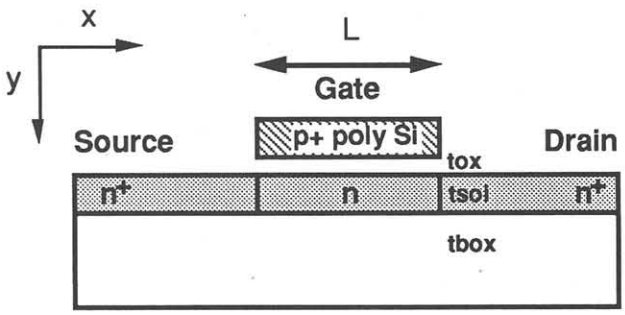

Fig. 1 Cross section of the investigated structure

channel AM MOSFET is considered with a p+ poly-Si gate. The channel doping is n-type resulting in an n^+-n-n^+ structure. The gate oxide and buried oxide thicknesses t_{ox} and t_{BOX} are fixed at 10nm and 380nm, respectively. Gate length L, SOI thickness t_{SOI} and channel doping N_D are varied. For the sake of simplicity interface traps and fixed oxide charges have been neglected. It has been shown that the AM SOI MOSFET exhibits a specific conduction mechanism consisting of two accumulation channels at front and back channel surfaces and a body current component[4,5]. The contribution of each to the total drain current depends on the device parameters and applied voltages. For zero back gate bias the potential in the SOI film has a maximum at the SOI/buried oxide interface (weak back accumulation[6]). Therefore, the threshold voltage (V_{th}) can be defined at the onset of accumulation at the back interface, i.e. the back surface potential ψ_b=0. The derived formula for the AM SOI

MOSFET threshold voltage is shown in eq. (1).

$$V_{th} = V_{FB}^{f} + \left(1 + 2\frac{C_{SOI}}{C_{OX}}\right)\frac{qN_D t_{SOI}^2}{2\varepsilon_{Si}} - \left(\frac{C_{BOX}}{C_{SOI}} + \frac{C_{BOX}}{C_{OX}}\right)\left(V_{SUB} - V_{FB}^{b}\right)$$
$$+\left(1 + \frac{C_{BOX}}{C_{SOI}} + \frac{C_{BOX}}{C_{OX}}\right)\frac{\psi_b - 2SH\left(2SH\left(\varphi_{bi} + V_D/2\right) + \sqrt{(\varphi_{bi} - \psi_b)(\varphi_{bi} + V_D - \psi_b)}\right)}{1 - 4SH^2} \qquad (1)$$

Thereby, C_{OX}, C_{SOI} and C_{BOX} are the capacitances of the gate oxide, SOI layer and buried oxide, respectively, ϕ_{bi} is the built-in potential of the source/channel junction, SH describes the short channel effect and is given by

$$SH = \frac{\sinh(L^*/2)}{\sinh(L^*)} \qquad (2)$$

with

$$L^* = L\sqrt{\frac{2\left(1 + \frac{C_{BOX}}{C_{SOI}} + \frac{C_{BOX}}{C_{OX}}\right)}{t_{SOI}^2\left(1 + 2\frac{C_{SOI}}{C_{OX}}\right)}} \qquad (3)$$

and the other symbols have their usual meanings. For increasing L^*, i.e. for large L and/or small t_{SOI}, SH approaches zero and eq. (1) reduces to the result of one-dimensional modeling[6].

RESULTS AND DISCUSSION

As illustrated in Fig. 2, the threshold condition ψ_b=0 holds true down to a certain channel doping level.

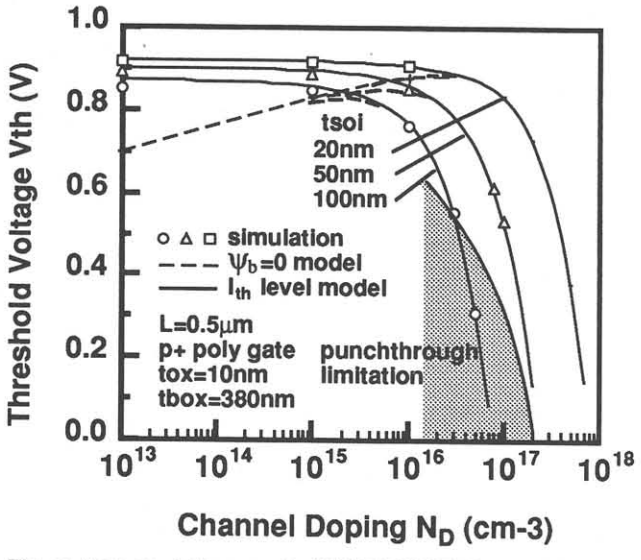

Fig. 2 Accumulation mode SOI MOSFET threshold voltage over channel doping

For smaller N_D the threshold voltage has to be defined at a threshold current level $V_{th}=V_G(I_{th})$ which requires a higher potential than ψ_b=0 in case of nearly intrinsic doping given in eq. (4).

$$\psi_b = \frac{kT}{q}\ln\frac{I_{th}}{kT\,\mu_n\left(1 - \exp(-qV_D/kT)\right)t_{SOI}N_D} \qquad (4)$$

with I_{th} = 0.1µA per unit W/L. Good agreement with simulation results is observed in Fig. 2. For increased doping N_D the AM MOSFET shows large back channel leakage current due to the loss of back potential control by the front gate voltage. The indicated punchtrough limitation in Fig. 2 is defined for the corresponding N_D where ψ_b cannot be reduced sufficiently to reach deep depletion at the back channel/oxide interface which is necessary to suppress the leakage current. Therefore, to obtain a useful V_{th} (e.g V_{th}=0.6V in the 0.5µm regime) the SOI thickness t_{SOI} has to be reduced. In the required doping range, however, V_{th} is very sensitive to doping fluctuations. It can be derived from eq. (1) and the corresponding expression for the inversion mode threshold voltage that the AM SOI MOSFET is inherently more sensitive to doping (N_D), substrate voltage (V_{sub}) and SOI thickness (t_{SOI}) variation than its IM counterpart by the factors given in eqs. (5) - (7).

$$\frac{\partial V_{th}^{acc}}{\partial N_D} = -\left(1 + \frac{1 + \frac{C_{OX}}{C_{SOI}} + \frac{C_{OX}}{C_{BOX}}}{1 + 2\frac{C_{SOI}}{C_{BOX}}}\right)\frac{\partial V_{th}^{inv}}{\partial N_A} \qquad (5)$$

$$\frac{\partial V_{th}^{acc}}{\partial V_{SUB}} = \left(1 + \frac{1 + \frac{C_{OX}}{C_{SOI}} + \frac{C_{OX}}{C_{BOX}}}{\frac{C_{SOI}}{C_{BOX}}}\right)\frac{\partial V_{th}^{inv}}{\partial V_{SUB}} \qquad (6)$$

$$\frac{\partial V_{th}^{acc}}{\partial t_{SOI}} = \left(1 + \frac{\left(1 + 2\frac{C_{OX}}{C_{SOI}}\right)\left(1 + \frac{C_{BOX}}{C_{SOI}}\right)^2 - 1}{\left(1 + \frac{C_{BOX}}{C_{SOI}}\right)^2 + 1}\right)\frac{N_D}{N_A}\frac{\partial V_{th}^{inv}}{\partial t_{SOI}} \qquad (7)$$

Eq. (7) is also valid in case of partial back depletion[6] where the potential maximum occurs inside the SOI film resulting in a body current. Fig. 3 illustrates eq. (7) and clearly shows that the lower sensitivity of the AM transistor to t_{SOI} variations stated as advantage of this transistor type in the literature is only due to the doping level differences required for a certain V_{th} because high p-type channel doping N_A is necessary for an n-channel IM SOI MOSFET with n^+-poly gate.

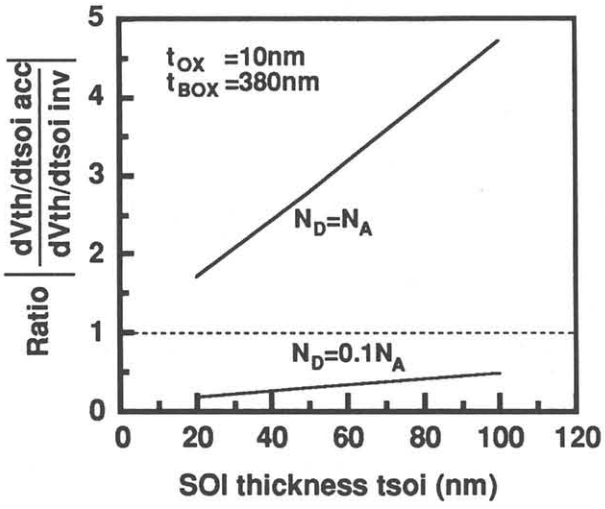

Fig. 3 Ratio of threshold voltage sensitivity on SOI thickness variation for AM and IM SOI MOSFET in dependence on tsoi and N_D

Generally, for smaller gate length down to 0.1μm low supply voltage will be mandatory. This demands low V_{th} and steep subtreshold slope (low S-factor) in order to ensure low leakage current as well as sufficient current drivability. Therefore, V_{th} control is then less governed by doping variation but by the gate workfunction. Suitable values can be achieved by using a metal silicide gate with a workfunction similar to intrinsic silicon (e.g. $MoSi_2$). Fig. 4 demonstrates the threshold voltage variation of the metal gate accumulation mode SOI MOSFET with gate length calculated by using eq. (1). Numerical simulation results are added for comparison.

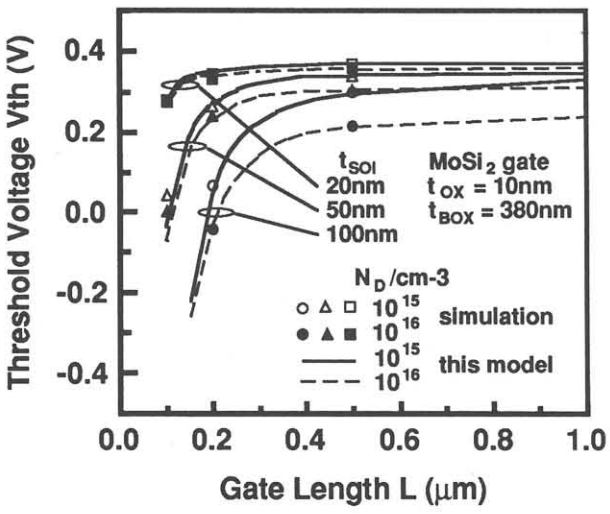

Fig. 4 Metal gate accumulation mode SOI MOSFET threshold voltage over gate length

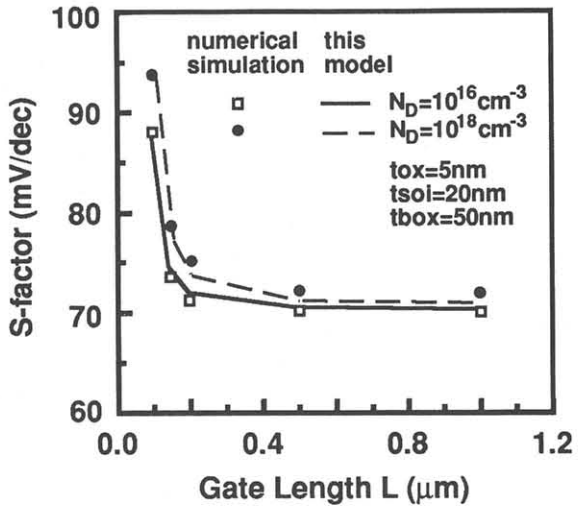

Fig. 5 Subthreshold slope vs gate length for accumulation mode SOI MOSFET

It can be seen that the key factor for the suppression of short channel V_{th} roll-off is the reduction of the SOI thickness t_{SOI}. Variation of the channel doping concentration N_D has only minor influence.
Furthermore, it must be noted in Fig. 5 that the strong degradation of the subthreshold slope at 0.1μm gate length cannot be reduced for the AM SOI MOSFET by increasing the channel doping concentration. This has been shown to be possible in case of the IM SOI MOSFET[1]. Even in the long channel region the S-factor of the accumulation mode transistor is increased due to body or back surface current flow.

CONCLUSION

The short channel behavior of accumulation type SOI MOSFETs has been investigated by means of a two-dimensional analytical model and numerical device simulation. It is found that the AM SOI MOSFET is more sensitive to parameter variations than its inversion mode counterpart. Key factor for suppression of short channel degradation is the thickness of the SOI layer. The effect of improvement of subthreshold slope by increasing the channel doping level does not exist for the AM SOI MOSFET.

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