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A Simple Method for Analyzing Bulk Versus Surface Punchthrough Current

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A simple methodology to study the origin of drain to source punchthrough leakage current will be presented. This technique is based on a capacitance model which allows the approximation of the depth at which the drain current flows for various bias conditions. The model has been verified using two dimensional device simulations. The methodology is demonstrated on a deep submicron n-channel MOSFET. The technique is relatively simple and requires only DC measurements.

1. Introduction

The need to improve circuit performance and packing density requires the continued reduction of MOSFET physical dimensions. As the MOSFET channel length is reduced the subthreshold or punchthrough leakage current will become the primary limiting factor. In order to design and analyze submicron devices the nature and location of the leakage current, whether bulk or surface, must be known. Although subthreshold leakage current has been studied by a number of authors [1-4], no simple method for analysis has yet been presented. It is the purpose of this paper to describe a simple method for analyzing punchthrough current.

2. Discussion

The minimum usable channel length of a CMOS technology is usually determined by the drain leakage current at Vg=0 volts and Vd=Vcc (figure 1). The subthreshold swing also deteriorates with decreasing channel length as shown in figure 2. To assist in further device optimization , it is useful to know if the leakage current is a surface current or a bulk current and the approximate depth of the current. This knowledge will suggest the appropriate design approach.

As indicated by Eitan and Frohman-Bentchkowsky[2], the origin of the punchthrough leakage current can be determined by the relative sensitivity of the leakage current to gate and body bias. Figure 3 shows the subthreshold leakage characteristics for a W/L=20/0.55um n-channel MOSFET. It is evident that the gate bias can significantly affect the leakage current. Similarly, figure 4, shows the effects of applied body bias on the leakage current .

In this work a simple capacitance model, shown in figure 5, is used to describe the coupling of the gate and body potentials to the point of maximum potential barrier height along the current path. A first order voltage divider allows the gate and body capacitances to be described as -

$$Cg = Ct\ (dVm/dVg) \quad \text{and} \quad Cb = Ct\ (dVm/dVb)$$

where Ct is the total capacitance, Vm is the barrier height, and Vg and Vb are the respective bias values. By using the expression Ids=A(exp(-q(Vm-Vs)/KT)) for the drain current, the capacitance ratio (Cg/Cb) can be written as

$$Cg/Cb = \frac{dLn(Ids)/dVg}{dLn(Ids)/dVb} \qquad (1)$$

Through the use of simple geometric expressions the capacitance ratio can be express as

$$Cg/Cb = \frac{td - tl}{tl - 3tox} \qquad (2)$$

where td, tl, and tox are dimensions defined in figure 5. The factor of three multipling the tox dimension is the ratio of the relative dielectric constants of silicon and silicon dioxide. This series of equations can be used to give an approximation of the depth at which the drain current flows if values of tox and td are known.

3. Results

Two dimensional simulations were used to verify the capacitance coupling model. The Cg/Cb ratio was calculated using equation 2 and simulated currents. Figure 6 shows the simulated Cg/Cb ratio versus Vgs at various Vds values for an n-channel MOSFET with a drawn channel length of 0.5um. The Cg/Cb ratio tends

to saturate as Vgs rises toward the threshold voltage. According to equation 2 the ratio should saturate when tl=0 (when the current flow is at the surface). The gate oxide thickness (tox) used for the simulations was 135 angstroms. The value of td was estimated from the saturation value of Cg/Cb. With both td and tox known, equation 2 can translate figure 6 into a plot of tl versus Vgs. This is shown in figure 7.

The 5 volt Vds curve in figure 7 shows tl to be very close to zero for Vgs>0.2 volts and approximately 3500 angstroms for Vgs<-0.2 volts. This is in reasonable agreement with the current density plots shown in figures 8a and 8b. Figure 9 is a plot of the current density versus depth at the center of the channel. There are two peaks in the current density, at the surface and in the bulk. The depth of the bulk path is in reasonable agreement with the saturation value of the depth for negative Vgs in figure 7.

The Cg/Cb ratio was determined for the technology featured in figures 1 to 4. The ratio was deduced from Ids(Vgs,Vbs) measurements and is shown figure 10. The similarity with the simulated curve shown in figure 7 is obvious. Using equation 2 and a gate oxide value of 135 angstroms, the depth of the current was calculated and is shown in figure 11. The bulk punchthrough path appears quite deep, suggesting the location for a punchthrough implant or well doping level adjustment. It should also be noted that at Vgs=0 volts and Vds=5 volts, the average depth of the incremental current is basically located at the surface. This surface current can be effectively reduced by adjusting the threshold voltage upward.

4. Conclusions

A simple methodology to study the origin of drain leakage current has been presented. It is based on a capacitance model which allows approximation of the depth at which the drain current flows for various bias conditions. The technique is relatively simple and requires only DC measurements.

5. References

[1] R.Troutman, IEEE Trans Elec Dev 26(1979) 461
[2] B.Eitan, et al, IEEE Trans Elec Dev 29(1982) 254
[3] J.S.Fu, IEEE Trans Elec Dev 31(1984) 440
[4] J.Pimbley, et al, IEEE Elec Dev 36(1989) 1711

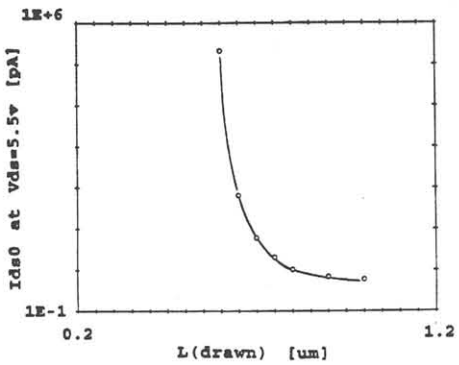


Fig.1 Ids0 at Vds=5.5 volts versus drawn gate length for an n-channel MOSFET.

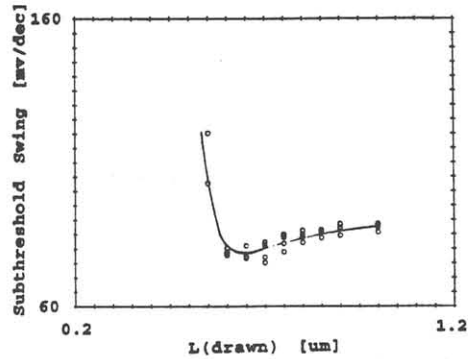


Fig.2 Subthreshold Swing versus drawn gate length for an n-channel MOSFET.

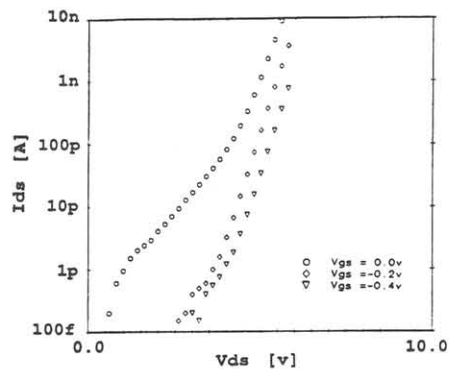


Fig.3 Ids versus Vds for various Vgs values with Vbs=0 volts.

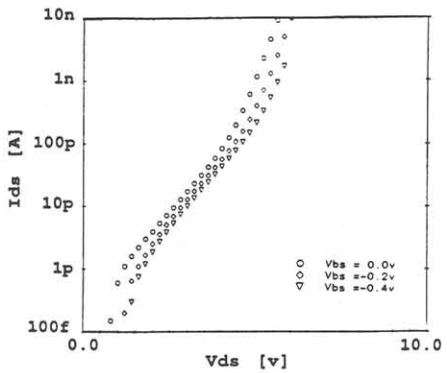


Fig.4 Ids versus Vds for various Vbs values with Vgs=0 volts.

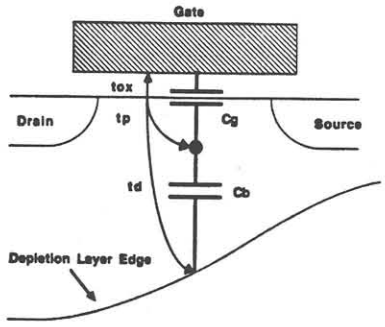


Fig. 5 Cross sectional diagram of an n-channel the definitions of model dimensions.

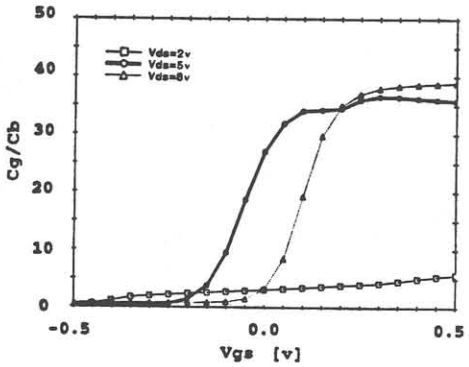


Fig.6 Simulated Cg/Cb versus Vgs for various Vds values.

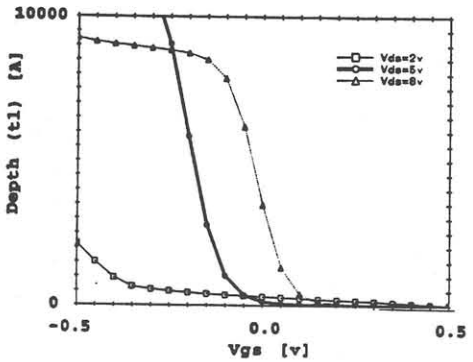


Fig.7 Calculated depth (based on simulations) of drain current flow versus Vgs for various Vds values.

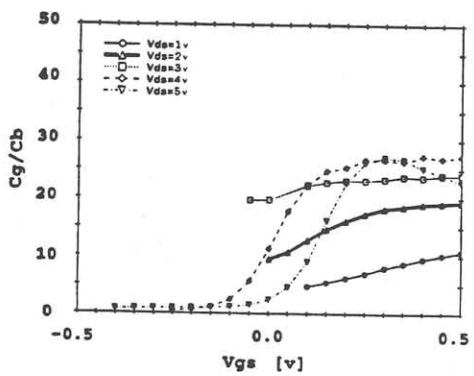
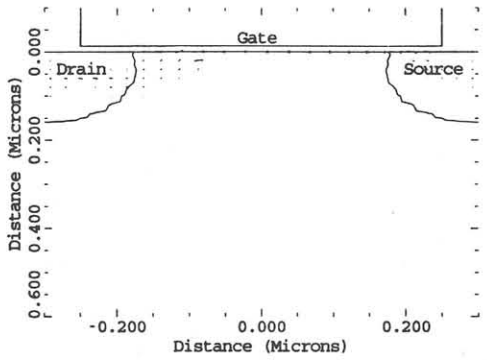
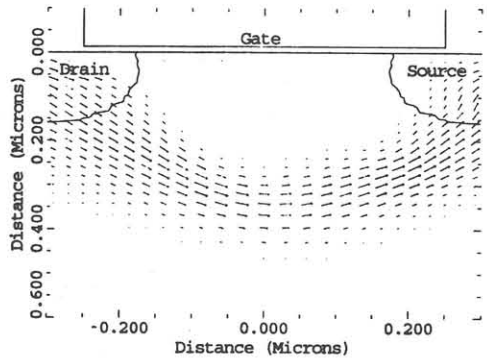


Fig.10 Measured Cg/Cb versus Vgs for a W/L=20/0.55 n-channel MOSFET.



(a)



(b)

Fig.8 Current flow for an n-channel MOSFET with drawn channel length of 0.5um for Vds=5 volts and (a) Vgs=0.6 volts and (b) Vgs=-0.3 volts.

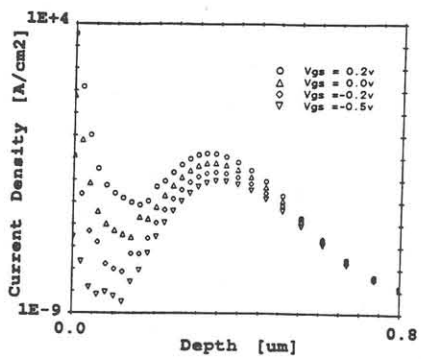


Fig.9 Simulated current density versus depth in silicon for various Vgs values.

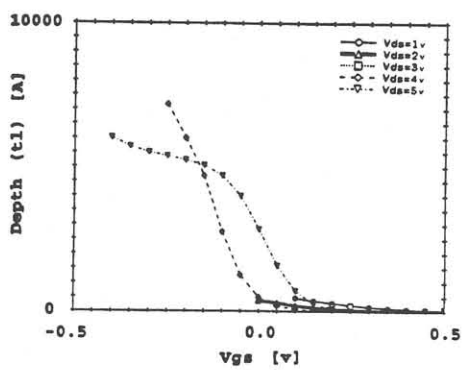


Fig.11 Calculated depth versus Vgs for a W/L=20/0.55um n-channel MOSFET