Extended Abstracts of the 1993 International Conference on Solid State Devices and Materials, Makuhari, 1993, pp. 491-493

PB-3-16

Low On-Resistance High-Voltage Power DMOSFET with an Interdigitated Form

Naoto Fujishima, Akio Kitamura, Gen Tada*

Fuji Electric Corporate Research and Development, Ltd.,
*Fuji Electric Co., Ltd.
4-18-1, Tsukama, Matsumoto City, 390, Japan

Abstract

This paper reports on a low on-resistance and high-voltage power DMOSFET with a newly proposed interdigitated form for power ICs, which are fabricated by cost-effective standard CMOS process. The basic structure has a highly doped drift region by forming an extended p-base in the drift region. In an interdigitated form for high current applications, the widely-spread depletion layer from the drain side avoids electric field concentration at the tip of the drain fingers. As for the tip of the source fingers, the newly proposed structure with a remainder p-substrate realizes a considerable decrease in electric field by charge sharing effect. The developed technology realizes a 2 A, 700 V power DMOSFET, whose specific on-resistance is 0.55 Ω · cm².

Introduction

In recent years, the technology of high-voltage integrated circuits have generated dramatic improvements. One way to enhance the voltage handling capability of the lateral DMOSFET is the RESURF technique [1].

A drawback of the RESURF technique is the high on-resistance of the transistors fabricated on thin epitaxial layers.

Another drawback is that since RESURF devices have interdigitated layouts for high current applications, electric field concentration, due to a small radius of curvature at the tip of each finger, limits breakdown voltage. On the other hand, large radius of curvature at the tip of them leads to the reduction in packing density, which increases the specific on-resistance.

In this paper, we will first propose a high-voltage device structure for the on-resistance reduction and show the devices characteristics at the portions which have corners with small radius of curvature. Next, we will explain the design concept and experimental results on a newly proposed structure which realizes an electric field reduction at the tip of the fingers in an interdigitated form.

Basic Structure

Fig. 1 and 2 show the top view of the DMOSFET in an interdigitated form, and the cross-section of the basic structure, respectively. The DMOSFET is fabricated by 2 μ m rule CMOS process on a high resistivity p-type substrate. The DMOSFET is formed in a n-type region which is formed by the n-well diffusion for low-voltage CMOS. An extended p-base with shallow junction is formed in the n-well. The basic structure consists of three parts. "A" is corresponding to the DMOS part which controls the current. Applied voltage is supported by "B" in the forward blocking state. "C" has a heavily doped n-type region for drain contact. When the device turns on, electron current from the source goes across the channel and flows into the n-well under the extended p-base to the drain. The aim of the device optimization is to minimize device on-resistance and chip area by achieving the required 700V blocking capability with the largest possible charge at the drift region and the shortest possible length in the three parts.

In the blocking state, the voltage, where depletion layer spreads in the extended p-base, is written as

$$V_{EP} = \frac{q}{2\varepsilon_0 \varepsilon_{Si}} X_{EP}^2 N_{EP} \left(1 + \frac{N_{EP}}{N_{WELL}}\right) \quad (1)$$

where X_{EP} is the depth of the extended p-base (cm);
N_{EP} is the average doping concentration of the extended p-base (cm^{-3});
N_{WELL} is the average doping concentration of the n-well (cm^{-3}).

On the other hand, the voltage, where the n-well is depleted, is given by

$$V_{WELL} = \frac{q}{2\varepsilon_0 \varepsilon_{Si}} X_{WELL}^2 N_{WELL} \left(1 + \frac{N_{WELL}}{N_{EP}}\right) \quad (2)$$

where X_{WELL} is the width of the n-type region between the p-substrate and the extended p-base (cm).

These relations follow directly from the one-dimensional Poisson equation upon application of the classical depletion approximations.

Both equations indicate that the smaller the product $X_{EP}^2 N_{EP}$ or $X_{WELL}^2 N_{WELL}$ is, the voltage V_{EP} or V_{WELL} is reduced under the condition where the magnitude of N_{EP} and N_{WELL} are almost the same. For instance, when N_{EP} and N_{WELL} are 10^{16}cm^{-3}, and X_{EP} and X_{WELL} are 1~2 μ m, V_{EP} and V_{WELL} become several tens of volts. This estimation indicates that even though the regions have high doping concentration, they are depleted at a low applied voltage.

The behavior for the depletion region and the way the electric field is reduced, are calculated by a two-dimensional device simulator. Fig. 3 shows the relationship between the impurity concentration of the extended p-base and the breakdown voltage. The result says that there is an optimum condition for the impurity concentration. If the concentration is higher than the optimum condition, breakdown voltage is limited at the drain side in the region "B". While, if the concentration is lower, it is limited at the

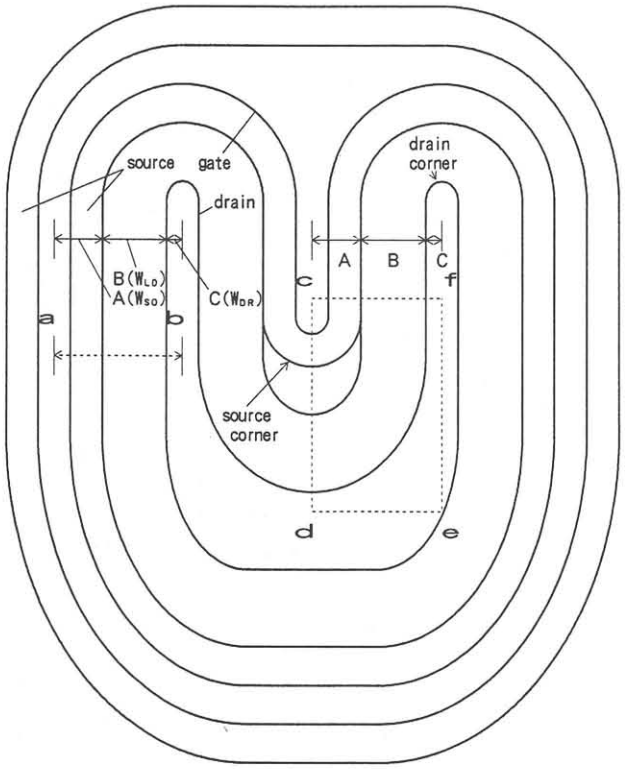

Fig. 1) Top view of the DMOSFET with an interdigitated form.

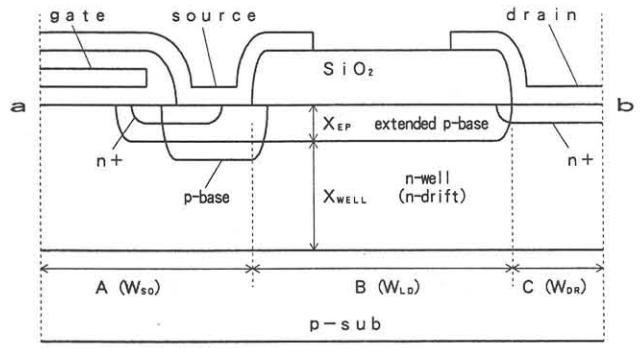

Fig. 2) Cross-section of the basic device structure.

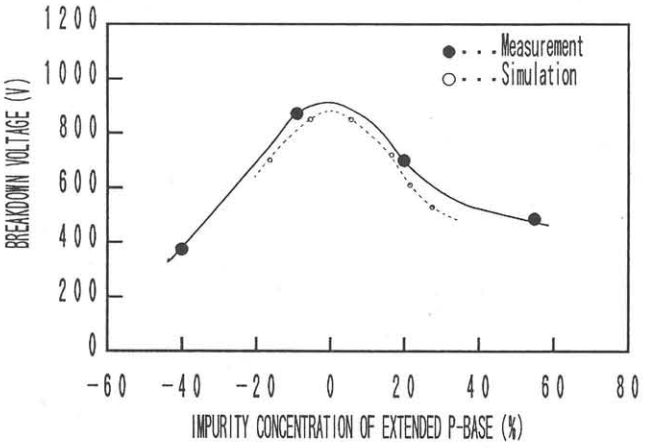

Fig. 3) Dependence of breakdown voltage on the impurity concentration of the extended p-base. The horizontal axis shows the rate of the deviation from the optimum condition.

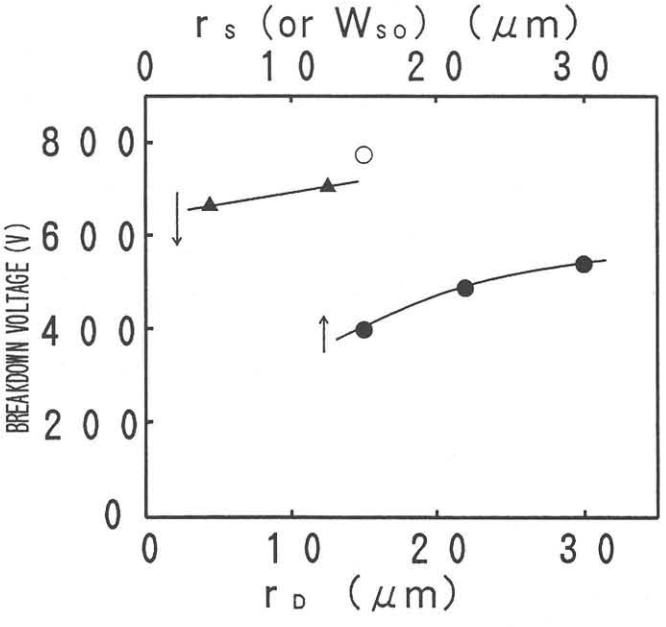

Fig. 4) Dependence of breakdown voltage on the radius of curvature at the tip of the drain (r_D) and source (r_S) fingers. The sign "○" shows the data for the device with the remainder p-substrate at the tip of the source finger.

source side. The structure with the extended p-base in the n-well realizes the drift region charge of 2.4×10^{12} cm^{-2} which is about three times larger than that for the conventional RESURF structure.

Experimental results are also plotted in Fig. 3. The agreement between experimental and simulated characteristics is very good. The experimental result shows that the DMOSFET with the basic structure has a BV_{DSS} of 880V and an on-resistance active area product of 0.35 Ω · cm^2.

Breakdown at the Corner

Interdigitated layouts are introduced to transistors to deal with a high current application. However, one concern is that the small radius of curvature in each finger might reduce the breakdown voltage.

Fig. 4 shows the dependence of the breakdown voltage on the radius of curvature at the tips of the drain (r_D) and source (r_S) fingers under the optimum condition. An interesting fact is that the breakdown voltages at the drain fingers are higher than at the source. In addition, the gradient at the drain finger (5 V/ μ m) is much smaller than that at the source (10 V/ μ m).

According to the two-dimensional device simulation for the basic structure, the depletion region in the extended p-base spreads at a lower voltage than in the n-well. The voltages are 20 V and 60 V for the extended p-base and the n-well, respectively. In the drain finger, since the depletion layer in the extended p-base widely spreads from the drain side at a lower drain voltage, larger effective radius of curvature avoids the extreme electric field concentration due to a reduction in r_D, which would be expected in the cylindrical junction model . Whereas, at the tip of the source finger, since the

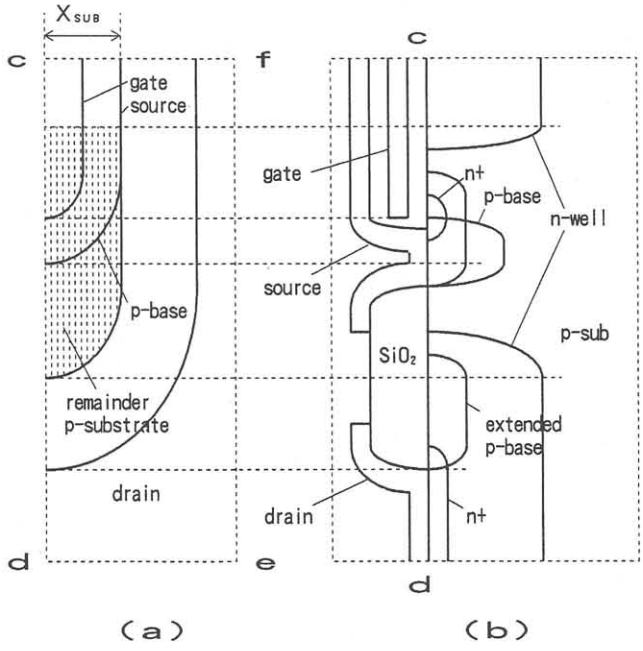

Fig. 5) Top view (a) and cross-sectional view (b) at the source corner including the newly proposed structure. The dotted region corresponds to the remainder p-substrate.

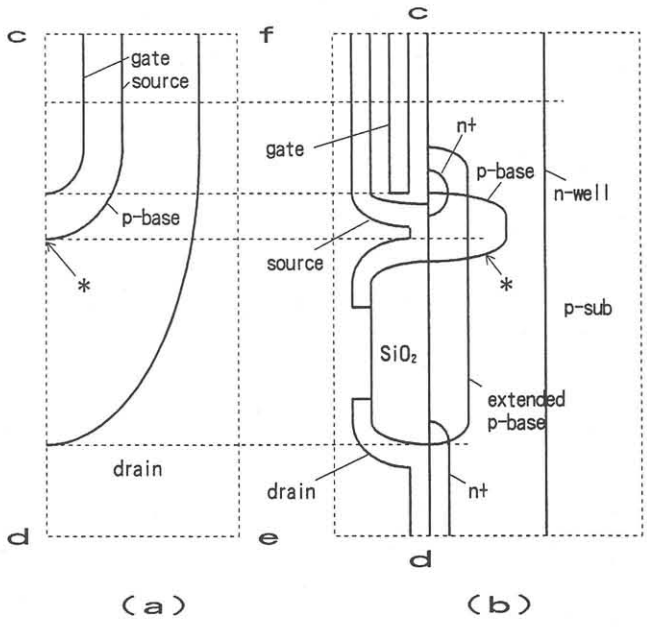

Fig. 6) Top view (a) and cross-sectional view (b) at the conventional source corner.

depletion region in the n-well spreads from the source side at a higher voltage than in the extended p-base, the depletion behavior is more similar to the cylindrical junction model. This reduces the breakdown voltage considerably as compared with the drain finger.

Electric Field Reduction at the Corner

Finally, the structure for reducing the electric field concentration at the tip of the source finger, is explained as follows. Fig. 5 and 6 show the top views (a) and the cross-sectional views (b) of the newly proposed and the conventional structures of the tips at the source fingers, respectively. In the case of the conventional structure shown in Fig 6, electric field at the outer corner of the p-base under the extended p-base concentrates at the point marked by " * ", due to a small radius of curvature at the corner. This limits breakdown voltage at a lower value. On the other hand, the newly proposed structure with the remainder p-substrate shown in Fig. 5, where n-well ion-implantation is not performed, has no p-n junction between the p-base and the n-well at the tip of the source finger.

When the horizontal view is taken instead of the vertical, the applied voltage, where the depletion region spreads in the remainder p-substrate, is given by

$$V_{SUB} = \frac{q}{2\varepsilon_0\varepsilon_{Si}} X_{SUB}^2 N_{SUB}\left(1+\frac{N_{SUB}}{N_{WELL}}\right) \qquad (3)$$

where X_{SUB} is one half of the width of the remainder p-substrate;

N_{SUB} is the average doping concentration of the p-substrate.

Since the remainder p-substrate has low impurity concentration and the area is surrounded by the n-well, the depletion region horizontally spreads from the junction between the remainder p-substrate and the n-well toward the remainder p-substrate at a low drain bias. For instance, when X_{SUB} and N_{SUB} are 15 μ m and 10^{14} cm^{-3}, respectively, V_{SUB} equals 17 V. And being helped by charge sharing effect, the newly proposed structure greatly reduces the electric field [2].

As shown in Fig. 4 marked by "○", although the width of part "A", W_{SO}, is only 15 μ m (which is corresponding to r_S=15 μ m), the corner does not limit the BV_{DSS} at all in the DMOSFET with the interdigitated form. It has successfully obtained a BV_{DSS} of 700 V and an on-resistance total device area product of 0.55 Ω · cm^2.

Conclusions

A low on-resistance, high-voltage DMOSFET for high current applications in a standard CMOS process has been developed. The charge sharing effect between the extended p-base and the n-well gives the basic structure a drift-region charge of 2.4 × 10^{12} cm^{-2} which is about three times larger than that for the conventional RESURF structure.

In an interdigitated form, although the radius of curvature is small, breakdown voltage is kept high at the tip of the drain finger. On the other hand, a reduction in the radius leads to a greater decrease in the breakdown voltage of the source finger.

The newly proposed structure which has a remainder p-substrate at the tip of the source finger succeeds in a dramatic reduction in the electric field, being free from limiting the breakdown voltage.

Overall, a 2 A power DMOSFET with the newly proposed interdigitated form has obtained a BV_{DSS} of 700 V and a specific on-resistance of 0.55 Ω · cm^2.

References

[1] J. A. Appels et al., IEDM Tech. Dig., paper 10.1, pp. 238-241, 1979.

[2] M. F. Chang et al., IEEE Trans. on Electron Devices. Vol. ED-33 No. 12, pp. 1992-2001, 1986.