

A New Recessed Channel MOSFET with Selectively Halo-Doped Channel and Deep Graded Source/Drain

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To improve the performance and reliability of deep submicron MOS devices, we propose a Gate-Recessed MOSFET (GR-MOSFET) which has a selectively halo-doped recessed channel and a deep graded source/drain formed without counter-doping. The GR-MOS structure eliminates the tradeoff between DIBL and hot carrier effect which are most important to deep submicron devices design. It also reduces the V_T lowering effect and lateral electric field at the drain. The fabricated $0.25\mu\text{m}$ GR-MOSFET with a 10nm gate oxide has exhibited 15% higher transconductance, 10% increased saturation current at $V_D=V_G=3.3\text{V}$, 1V higher BV_{DSS} and 6 times less substrate current compared with a LDD-MOSFET of same device dimension.

1. INTRODUCTION

To improve the circuit performance, the device feature size reduction is essential. However, as MOS devices are scaled down to deep submicron regime, undesirable side-effects such as the off-state leakage by the DIBL (drain-induced barrier lowering), the hot carrier induced device degradation, the short channel effect and the avalanche induced source/drain breakdown are encountered. These problems are related to the channel and the source/drain doping profile of the conventional MOS structure. In this paper, we propose a new gate-recessed channel MOSFET (GR-MOSFET) [1] with selectively halo-doped channel and deep graded source/drain doping profile to improve the short channel effects, the hot carrier effect, the punchthrough and the current drivability, and present some characterization results of GR-MOSFET with a $0.25\mu\text{m}$ gate length in comparison with a conventional LDD-MOSFET of the same gate length.

2. EXPERIMENTS

Fig. 1 shows the cross section of a GR-MOSFET. The key process sequence different from a conventional LDD fabrication can be described as follows. After forming the LOCOS, the thick Si_3N_4 film was removed and a thin film of Si_3N_4 (75nm) was redeposited. The channel region was defined by electron-beam lithography and the nitride film on this channel area was etched away. A 350nm oxide (gate recess oxide) was grown in order to recess the channel and use as a self-aligned mask for the source/drain implantation.

Phosphorus of $1 \times 10^{15} \text{cm}^{-2}$ was then implanted at an energy of 110keV that allows the dopant to penetrate into S/D region only, not into the channel region covered with a 350nm SiO_2 . Reactive ion etching with a high selectivity to a Si_3N_4 was performed to etch the 350nm gate recess oxide with the existing nitride as a mask to open the channel region. The bird's beak oxide at S/D edges covered with the Si_3N_4 remained only. Then, the BF_3 implantation of a $2 \times 10^{12} \text{cm}^{-2}$ dose was carried out at 50kV to adjust threshold voltage and $3 \times 10^{13} \text{cm}^{-2}$ boron ions were implanted to prevent the punchthrough, and followed by a 10nm gate oxidation. The bird's beak oxide plays an important role in forming the graded and sloped S/D junction, introducing a selectively halo-doping in the channel region (Fig. 2(a)). From the gate oxidation, the rest of processes is same as the conventional MOS fabrication procedures.

Fig. 2. shows the final impurity profiles for the typical GR-MOSFET and a conventional LDD-MOSFET. The starting material is a p-type (100)-oriented Si wafer with $8.5\text{--}9.5\Omega\cdot\text{cm}$ and the final S/D junction depth measured by ASR is $0.35\mu\text{m}$.

3. RESULTS and DISCUSSION

The concept of GR-MOSFET is to introduce the lower concentration doping profile at the channel and the S/D edges as shown in Fig. 2(a). It gives the punchthrough hardness by maintaining the built-in barrier at the source end even at the higher drain bias. By reducing the lateral electric field and also moving the electric field maximum point far into the drain, the electron temperature

and the hot carrier generation can be decreased as shown in Fig. 3 of MEDICI[2] simulation. From this result, GR-MOSFET structure is proven to be more efficient than LDD(lightly doped drain) or SD(single drain) structure at the deep submicron regime.

The fabricated samples were characterized and compared with the LDD device which has nearly identical dimensions($W_{eff}=18.9\mu m$, $L_{eff}=0.25\mu m$ and $T_{ox}=10nm$). In I_D-V_D curves of Fig. 4, several improvements of GR-MOSFET can be noticed: more than 1V increase in drain sustaining voltage(BV_{DSS}), excellent saturation characteristics up to $V_G=V_D=5V$ and 10% enhanced current drivability. The excellent saturation characteristics and the higher BV_{DSS} are due to the graded drain doping profile and the halo-doping profile of the channel at the source end which prevent drain field from penetrating into the channel. This also alleviates such short channel effect as V_T lowering(Fig.5) and DIBL(Fig.6). More than 10% increase in the saturation current and in the maximum transconductance(177mS/mm for GR-MOSFET and 155mS/mm for LDD-MOSFET at $V_D=4V$ and $L_{eff}=0.25\mu m$) are resulting from the lower S/D resistance(30 $\Omega/\square$ for GR-MOSFET, 40 $\Omega/\square$ for LDD-MOSFET). For the hot carrier characteristics, the measured substrate currents in Fig. 7 are about 6 times less than those of LDD-MOSFET. It is due to the one order of magnitude reduced electric field by the graded drain doping profile and clearly seen in I_{SUB}/I_D vs. $1/I_D$ plot[3] of Fig. 8.

4. CONCLUSIONS

In summary, GR-MOSFET of a new doping concept is fabricated by making the doping profiles near both channel ends gradually lower using the bird's beak oxide and verified that the new structure shows much more improved device characteristics, especially related to short channel effects and hot carrier effects and has a feasibility as a deep submicron MOS structure.

REFERENCES

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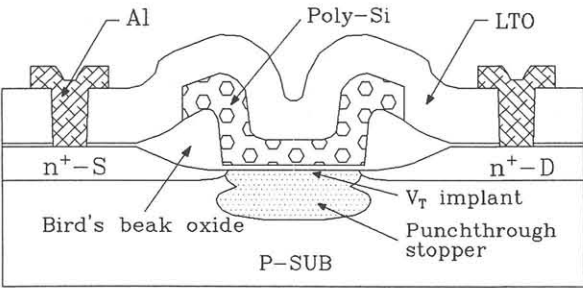
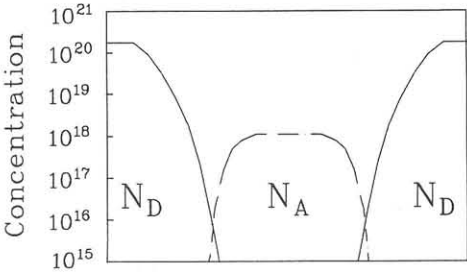
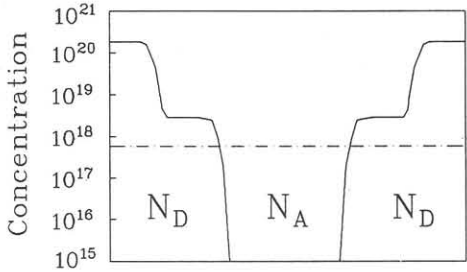


Fig.1. Cross section of GR-MOSFET structure.



(a) GR-MOSFET



(b) LDD-MOSFET

Fig.2. Schematic diagram of doping profile for (a) GR-MOSFET and (b) LDD-MOSFET.

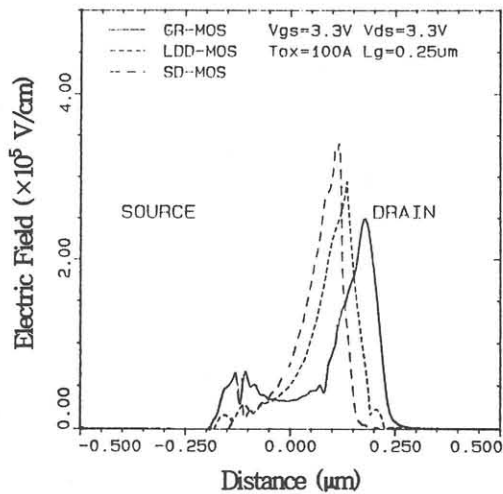


Fig.3. Lateral electric field simulation of GR, LDD, SD-MOSFET ($-0.125\mu\text{m} \leq \text{gate} \leq 0.125\mu\text{m}$).

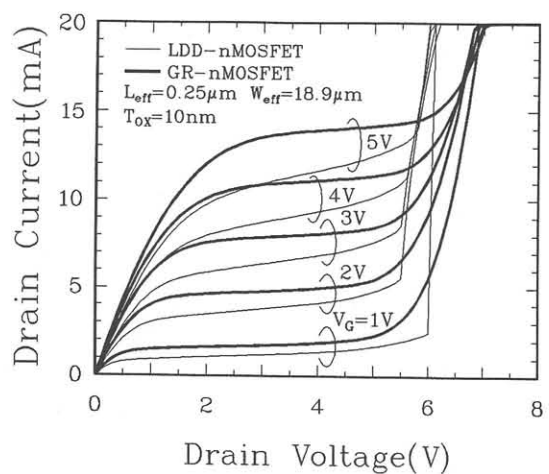


Fig.4. I_D - V_D characteristics of GR-MOSFET and LDD-MOSFET ($W_{\text{eff}}=18.9\mu\text{m}$, $T_{\text{ox}}=10\text{nm}$).

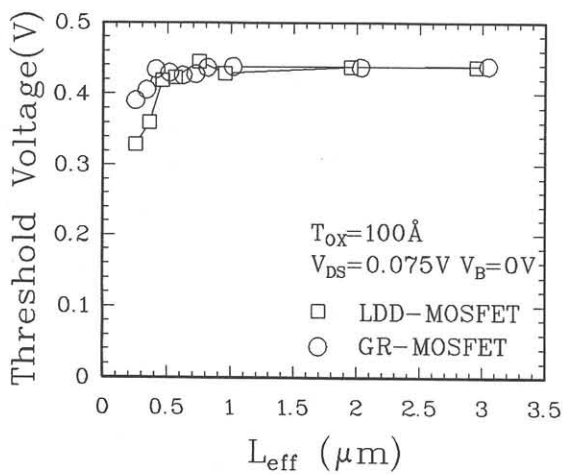


Fig.5. Threshold voltage lowering of GR-MOSFET and LDD-MOSFET.

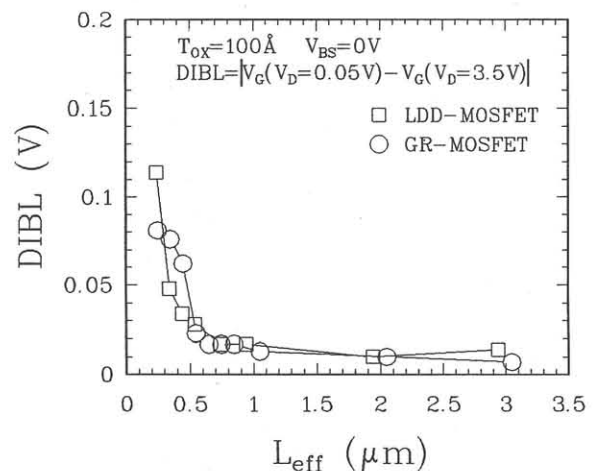


Fig.6. DIBL characteristics of GR-MOSFET and LDD-MOSFET at various effective channel length.

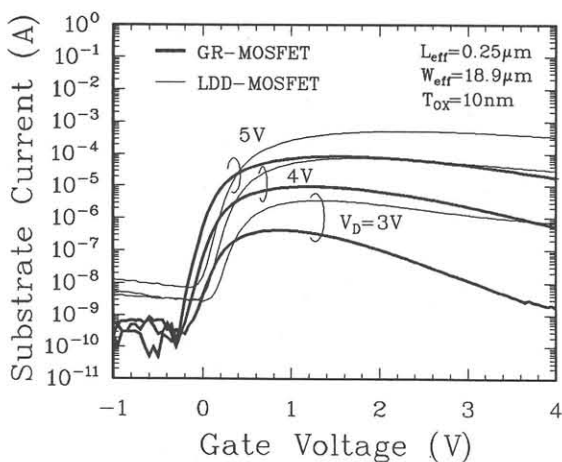


Fig.7. Substrate currents of GR-MOSFET and LDD-MOSFET.

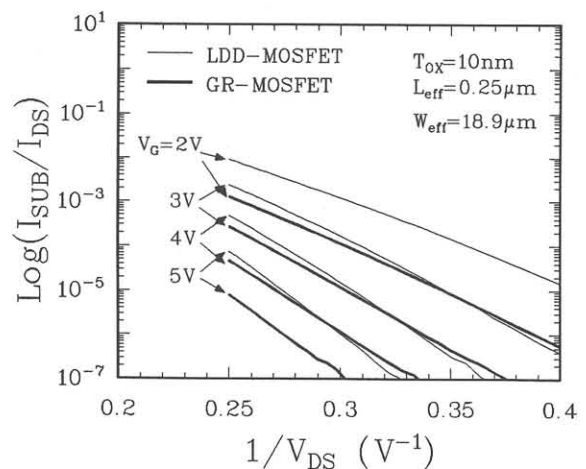


Fig.8. I_{SUB}/I_D characteristics of GR-MOSFET and LDD-MOSFET.