

Bipolar Transistor with a Buried Layer Formed by High Energy Ion Implantation for Sub-Half Micron BiCMOS LSI

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The buried layer formed by high energy ion implantation was used for bipolar transistor without increase in leakage current. Moreover, the maximum current gain of 155 and the cutoff frequency of 17.3 GHz were achieved with $BV_{CE0}=5.0$ V. The increase in collector resistance would be tolerable for low power applications. This fabrication process is applicable to the conventional CMOS process with the retrograde twin well without additional process steps. Therefore, this technique can be very promising for the sub-half micron BiCMOS LSI.

1. Introduction

BiCMOS technology has been attracting attention for use in high speed LSIs. However, the fabrication process of BiCMOS is usually very complicated in the conventional process where many process steps to form a buried layer are necessary employing epitaxial layer growth. As a result, considerable vertical and lateral impurity diffusion from the buried layer during the following high temperature heat treatment prevents miniaturization of device size. In addition, production cost becomes very high. High energy ion implantation techniques overcome these problems because the N^+ buried layer is directly formed after high temperature heat treatment without epitaxial layer growth.^{1,2)} In order to use this technique in the bipolar process, the leakage current related to the implantation damage must be reduced. In the high dose region, leakage current can be minimized by the self-gettering mechanism for the buried collector.³⁾ The increase in leakage current in the medium dose region for practical use remains a serious problem. However, the significant reduction in leakage current can be achieved by the rapid thermal annealing.⁴⁾ Here, we demonstrate the characteristics of bipolar transistors using the newly developed process technique which is compatible with the CMOS retrograde twin well without additional process steps.

2. Experimental

Figure 1 shows the fabrication process flow and the schematic cross-section of a bipolar transistor with a buried layer formed by high energy ion implantation. P-type $10\ \Omega\text{ cm}$ CZ silicon wafers were prepared for this experiment. To avoid the considerable out-diffusion of the buried layer, high temperature heat treatments employed for the LOCOS formation and the collector wall formation by phosphorus deposition were achieved at the first stage of process. The P^+ isolation region and the collector region were formed by the multiple high

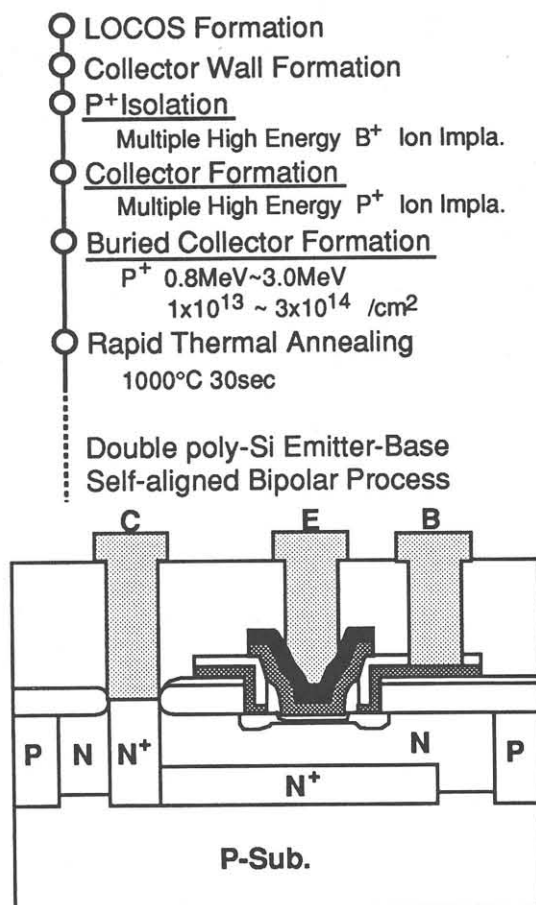


Fig. 1 Fabrication process flow and schematic cross-section of a bipolar transistor with a buried layer formed by high energy ion implantation

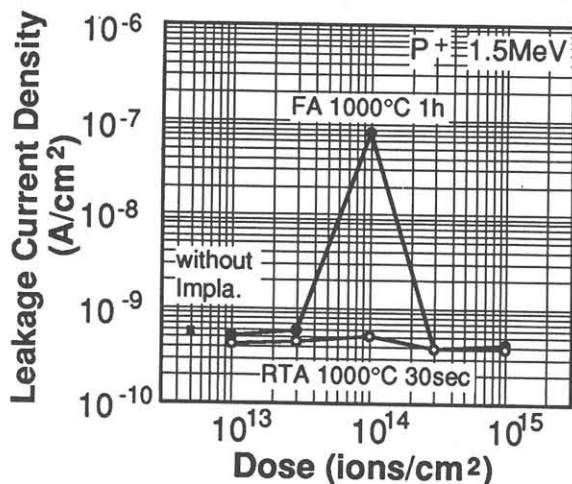


Fig. 2 Dependence of junction leakage current of diodes on phosphorus dose with annealing condition as a parameter

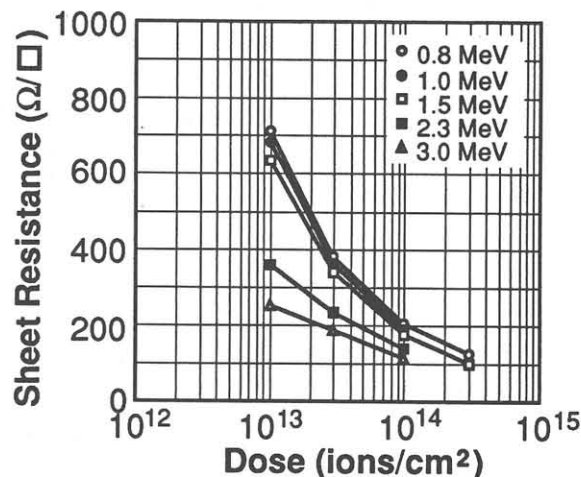


Fig. 4 Dependence of collector sheet resistance on phosphorus dose with implantation energy as a parameter

energy boron and phosphorus implantations, respectively. Subsequently, the N^+ buried layer was directly formed by the high energy phosphorus ion implantation with energies varying from 0.8 MeV to 3.0 MeV. The implantation doses were changed from the ranges of 1×10^{13} to $3 \times 10^{14} / \text{cm}^2$. Next, samples were annealed at 1000 °C for 30 sec by the rapid thermal annealing in order to reduce the leakage current. Both the lateral and the vertical diffusion of phosphorus can be effectively minimized by the small thermal budget after the implantation for a buried layer formation. Subsequently, the double poly-Si emitter-base self-aligned bipolar transistor was fabricated by the conventional bipolar process.⁵⁾

3. Results and Discussion

Figure 2 shows the leakage current of p^+/n junction at a reverse voltage of 5 V as a function of implantation dose for a buried layer formation. While the leakage current generally increased with increasing dose, a remarkable decrease in the leakage current is observed at around the dose of $3 \times 10^{14} / \text{cm}^2$ in the case of furnace

annealing. The reduction in the leakage current is attributed to the gettering of micro-defects by secondary defects induced by an implantation of dopant itself (self-gettering). In the case of the rapid thermal annealing, no increase in the junction leakage current can be observed. Therefore we use the rapid thermal annealing to recover the crystal damage as well as to activate dopants for practical production. Figure 3 shows the dependence of breakdown voltage between the collector and the base (BVC_{BO}) values on implantation dose as a function of implantation energy for the buried layer formation. BVC_{BO} values decrease with increase in implantation dose and increase with increase in implantation energy for the buried layer formation. Figure 4 gives the dependence of the collector sheet resistance on implantation dose with implantation energy for the buried layer formation as a parameter. The collector sheet resistance increases with decrease in implantation dose. The collector resistance value of $180 \Omega/\square$ is obtained in the case of 1.5 MeV phosphorus implantation with a dose of $1 \times 10^{14} / \text{cm}^2$. This value is about six times larger than the value in the conventional Sb^+ implanted buried layer with a silicon epitaxial layer.

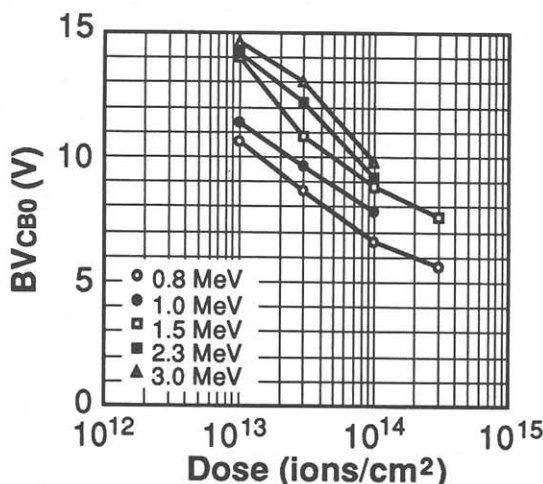


Fig.3 Dependence of BVC_{BO} values on phosphorus dose with implantation energy as a parameter

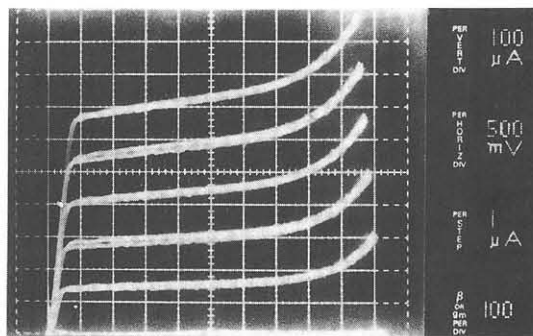


Fig. 5 I-V characteristic for NPN transistor with a buried layer formed by phosphorus implantation at 1.5 MeV at a dose of $1 \times 10^{14} / \text{cm}^2$

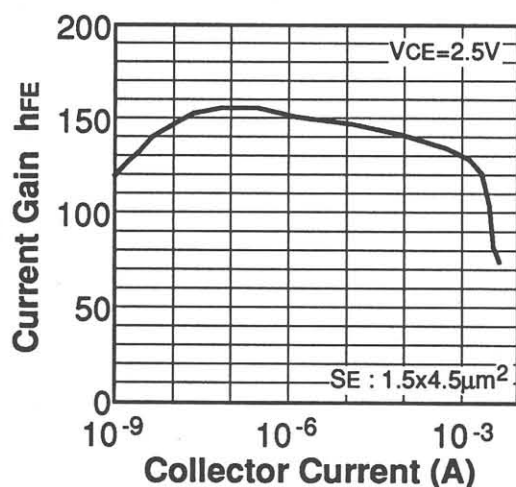


Fig.6 Current gain versus collector current for bipolar transistor measured on the same sample with fig.5

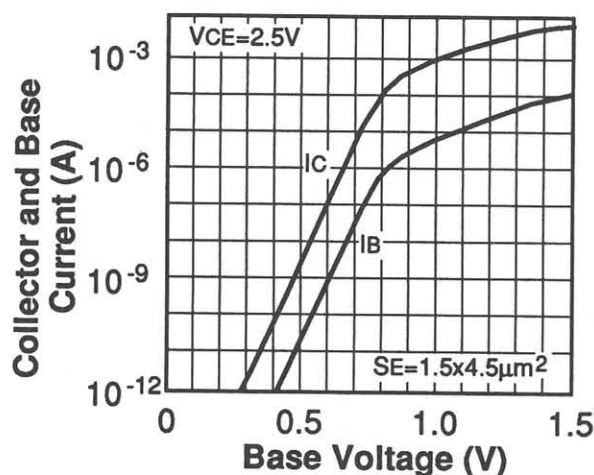


Fig. 7 Gummel plot of bipolar transistor measured on the same sample with fig. 5

Current amplification characteristics for a NPN transistor with $1.5 \times 4.5 \mu\text{m}^2$ emitter area is shown in figure 5. The buried layer was formed by phosphorus implantation at 1.5 MeV with a dose of $1 \times 10^{14} / \text{cm}^2$. The breakdown voltage between the collector and the emitter (BV_{CE0}) is 5.0 V. Current gain h_{FE} versus collector current is given in figure 6. The maximum current gain of 155 was achieved at the collector bias of 2.5 V. Nearly constant current gain over 6 decades of the collector current can be observed. Gummel plot of bipolar transistor is depicted in figure 7. No increase in recombination and generation current can be observed in the low current region. This result shows that defects formed through high energy ion trajectory can be recovered by the rapid thermal annealing. Figure 8 shows the dependence of cutoff frequency on collector current where the maximum cutoff frequency of 17.3 GHz was obtained due to a small capacitance between the collector and the base.

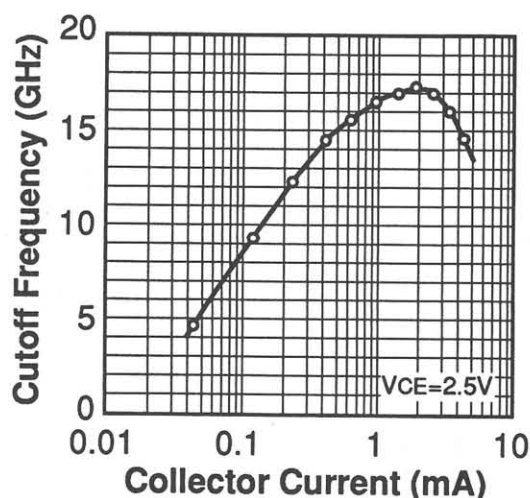


Fig. 8 Cutoff frequency versus collector current for bipolar transistor measured on the same sample with fig. 5

4. Conclusion

From our extensive investigation, we conclude that the buried layer formed by high energy ion implantation can be used for bipolar transistor without increase in leakage current. Moreover, the maximum current gain of 155 and the cutoff frequency of 17.3 GHz were achieved with $BV_{CE0}=5.0$ V. The increase in the collector resistance would be tolerable for low power applications. This fabrication process is applicable to the conventional CMOS process with retrograde twin well without additional process steps. ⁶⁾ Therefore, this technique can be very promising for the sub-half micron BiCMOS LSI.

5. Acknowledgement

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