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A Concise Analytical Model for Deep Submicron NMOS Devices Considering Energy Transport

S. Y. Ma and J. B. Kuo

Rm. 526, Dept. of Electrical Eng., National Taiwan University
Roosevelt Rd. Sec. 4, #1, Taipei, Taiwan 106-17
Fax:886-2-367-7214, Phone:886-2-363-5251 x285

This paper reports a concise analytical model for deep submicron NMOS devices considering energy transport. As verified by the experimental data, the analytical model shows a good accuracy in the IV characteristics.

Summary

Conventional drift-diffusion models are applicable for NMOS devices with a channel length down to $0.25\mu m$ [1]. For NMOS devices with a channel length less than $0.25\mu m$, the lateral electric field in the device can be large– the electric field affects the electron energy distribution. As a result, the electron temperature is much higher than the lattice temperature. Therefore, energy transport is also important in determining the current conduction of the device [2]. Under this situation, to obtain an accurate IV characteristics for the device, Boltzmann transport equations should also be solved simultaneously– analytical model is difficult to obtain. Consequently, 2D device simulation is necessary [3]-[5]. Incorporating the electron temperature effects including velocity overshoot [5] by modifying the conventional mobility model, analytical models for deep submicron NMOS devices have been reported [1][6]. In this paper, by directly simplifying the energy transport equation, a concise analytical model for deep submicron NMOS devices is reported.

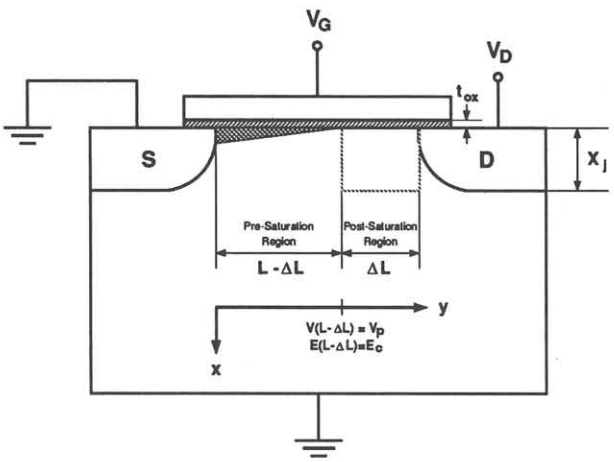

Fig. 1. Cross section of the deep submicron NMOS Device under study.

Consider an NMOS device with an effective channel length of $0.1\mu m$ as shown in Fig. 1. Energy balance equation is as shown Eqs. (1)(2) in Fig. 2. In the NMOS device, the electron current is mainly composed of drift current as shown in Eq. (3) From

1. $JE = nB(T_n) + \frac{dS}{dy}$
2. $S = -\kappa\frac{\partial T_n}{\partial y} - J\frac{kT_n}{q}\delta$
3. $J = nq\mu_n E$
4. $q\mu_n E^2 = B(T_n) - \mu_n \delta k E \frac{dT_n}{dy}$
5. $B(T_n) = q\mu_n(\frac{v_{sat}}{\mu_o})^2\frac{T_n - T_o}{T_o}$
6. $qE^2 = q(\frac{v_{sat}}{\mu_o})^2\frac{T_n - T_o}{T_o} - \delta k E\frac{dT_n}{dy}$
7. $T_n(y) = T_o + \frac{qT_oE_c^2\mu_o^2y^2}{2\delta E_c k\mu_o^2(L-\Delta L)+qv_{sat}^2(L-\Delta L)^2}$
8. $I_D = \mu_o C_{ox}\frac{W}{L-\Delta L}(V_G - V_T - \frac{V_p}{2})V_p$
   $(1 + \frac{qE_c^2\mu_o^2(L-\Delta L)}{6\delta k T_o E_c\mu_o^2 + 3qv_{sat}^2(L-\Delta L)})^{-1}$
9. $V_D = V_p + E_c\frac{\lambda^2}{L-\Delta L}(cosh\frac{\Delta L}{\lambda} - 1) + E_c\lambda sinh\frac{\Delta L}{\lambda}$

Fig. 2 Important Equations.

Eqs.(1)-(3), one obtains Eq. (4). Using Taylor's formula [7], the $B(T_n)$ in the $nB(T_n)$ term can be expressed as Eq. (5). From Eqs. (4)&(5), Eq. (6) is obtained. Using a similar approach as in the paper by El-Mansy et. al. [8], the lateral channel of the NMOS device is divided into two sections – the (1) pre-saturation region and (2) the post-saturation region, separated by the "saturation point", where its electric field is E_c and its channel potential is V_p. In the pre-saturation region, the electric field in the channel between source and the saturation point has been assumed to be linear. From Eq.(6), with the boundary condition – the electron temperature at source is equal to the lattice temperature ($T_n(0) = T_o$), the electron temperature at location y is obtained – Eq. (7). Using the temperature-dependent mobility formula [6], the drain current can be expressed as Eq. (8). In the post-saturation region, 2D Gauss' Law has been applied in the Gaussian box area as shown in Fig. 1 – from the saturation point to a location y before drain in the lateral direction and from oxide interface to the junction depth in the vertical direction. Solving this equation with boundary conditions at the saturation point, and Eq. (9) is obtained. From Eqs. (8)(9), the drain current model of the NMOS device considering energy transport has been derived.

In order to show the effectiveness of the analytical model, the analytical model results have compared to the experimental data [9]. The NMOS device under study has an effective channel length of $0.1\mu m$ and a gate oxide of $45\mathring{A}$ and a S/D junction of $650\mathring{A}$ and a substrate doping density of $3 \times 10^{17}cm^{-3}$. The zero bias threshold voltage of the device is $0.15V$. Fig. 3 shows the I_D vs. V_{DS} curves for the NMOS device biased at V_G of $0.8V$, $0.6V$, and $0.4V$ and V_D from $0V$ to $1V$. A good match between the analytical model results and the experimental data can be seen. For circuit applications, output conductance and transconductance are importance in determining the performance of an NMOS device. Fig. 4 shows the output conductance vs. V_{DS} for the NMOS device biased at $V_{GS} = 0.8V$, $0.6V$, $0.4V$ using the analytical model. Also shown in the figure are the results based on the model without considering energy transport. The result using the analytical model with energy transport is larger than that without it. Fig. 5 shows the transconductance vs. effective channel length of the deep submicron NMOS device based on the analytical model and the experimental data [10]. The NMOS device is biased at $V_{DS} = 0.8V$. Also shown in the figure is the model result without considering energy transport. The result using the analytical model with energy transport is smaller than that without it. The analytical model result considering energy transport shows a good match with the experimental data.

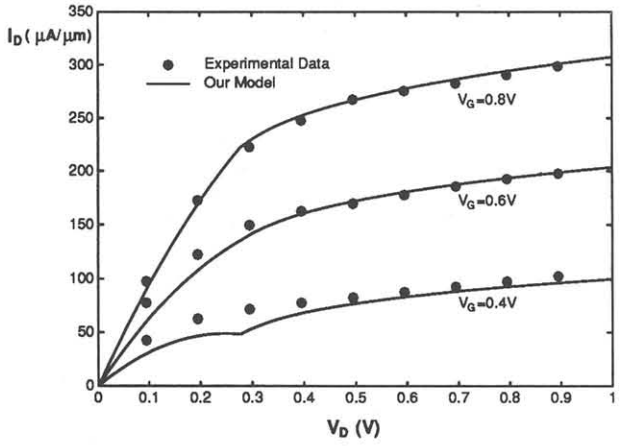

Fig. 3. The I_D vs. V_{DS} curves for the NMOS device with an effective channel length of $0.1\mu m$ and a gate oxide of $45\mathring{A}$ and S/D junction depth of $650\mathring{A}$ and a substrate of $3 \times 10^{17} cm^{-3}$, biased at V_G of $0.8V$, $0.6V$, and $0.4V$.

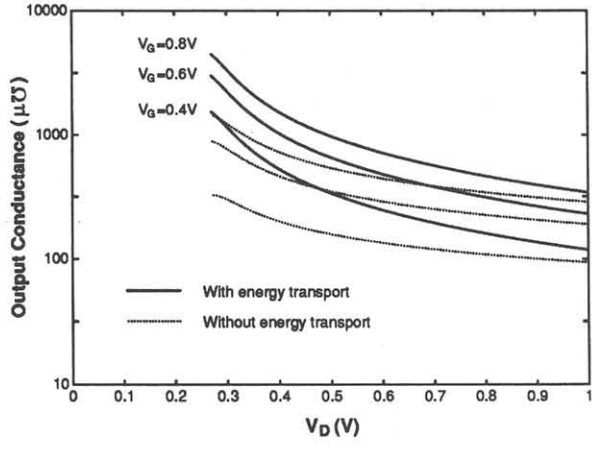

Fig. 4. The output conductance vs. V_{DS} of the $0.1\mu m$ NMOS device biased at $V_{GS} = 0.8V, 0.6V, 0.4V$

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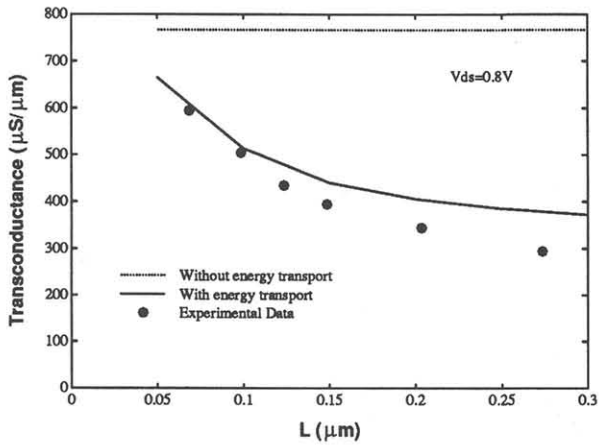

Fig. 5. The transconductance vs. effective channel length of the deep submicron NMOS device based on the analytical model and the experimental data. The NMOS device is biased at $V_{DS} = 0.8V$.

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