# Improvement of the Interface between Selectively Deposited Al and Si by Annealing

Kouichi TANI and Satoshi.NISHIKAWA

Semiconductor Tech. Lab., Oki Electric Industry Co., Ltd.

550-5 Higashiasakawa-cho, Hachiohji-shi, Tokyo 193, Japan

The interaction between Al deposited selectively by CVD and Si has been investigated. The structure of Al depended on the size of contact holes. Al was single-crystalline in  $0.7\mu$ m contact holes, but polycrystalline in  $1.2\mu$ m and  $2.0\mu$ m holes. In the case of single crystalline Al, Si at the bottom of contact holes was eroded uniformly by Al after deposition and after annealing at 400°C. In the case of polycrystalline Al, Si was eroded nonuniformly and Al spikes were formed. However, after annealing at 400°C, the Al spikes disappeared and the surface of eroded Si became extremely flat. Junction leakage current of the 2.0 $\mu$ m n<sup>+</sup> contact was found to increase after Al deposition. However, after annealing at 400°C, the increase of junction leakage current was not found to 10V. The change may be due to the improvement of the interface. These results indicate that selective Al-CVD can be used safely as a contact-hole-filling method.

# **§1** Introduction

In multilevel interconnections for ULSI, filling narrow holes of high aspect ratio has been one of the main difficulties. For this purpose, selective deposition of Al onto contact holes is very attractive and has been investigated by several researchers. In recent years, selective Al CVD has been achieved by controlling the deposition temperature.<sup>1)-3)</sup> However, in the case of filling holes by this method, an Al-Si direct contact was formed. It is well known that an interaction between Al and Si occurs in an Al-Si direct contact, i.e., Si is eroded by Al and Al spikes are formed.

In this study, we investigated the interaction between selectively deposited Al and Si and proposed a method for improving the interface between Al and Si.

## §2 Experimental conditions

Si(111) wafers with orientation of about 3° off-angle were used. These wafers were covered with SiO<sub>2</sub> films, and  $0.7\mu$ m,  $1.2\mu$ m, and  $2.0\mu$ m contact holes were formed. Before deposition of Al, the wafers were dipped in 1% HF solution for 45s and rinsed in deionized water. After these treatments, Al was deposited by low-pressure CVD using dimethylaluminum hydride (DMAH). The substrate temperature was 340°C and the deposition time was 60s. Under these conditions, Al was selectively deposited. After the deposition, these samples were annealed in H<sub>2</sub> ambient at 400°C for 30 min.

The morphologies of selectively deposited Al and the Si surface at contact holes were characterized by scanning electron microscopy (SEM) and atomic force microscopy (AFM). Electrical properties, such as junction leakage current and contact resistance, were measured using n+/p diodes whose junction depths  $(x_j)$  were 230nm and 330nm (simulated).

## §3 Results and discussion

# 3-1 Improvement of the Al-Si interface

Figure 1 shows the SEM photographs of selectively deposited Al and Si surface after removal of Al and SiO2 films by wet etching. After deposition, contact holes were completely filled with Al, as shown in Fig 1(a). The structure of Al depends on the size of holes. Al was single-crystalline in 0.7µm holes, but polycrystalline in 1.2µm and 2.0µm holes. Si at the bottom of holes was eroded laterally and vertically during deposition, as shown in Fig 1(b). The shape of holes became hexagonal for all sizes of holes. The behavior of vertical erosion depends on whether deposited Al is single crystalline or polycrystalline. In 0.7µm holes, Si was eroded uniformly, while in 1.2µm and 2.0µm holes, nonuniform erosion occurred and Al spikes were formed. The erosion pattern is similar to that at the grain boundary of Al. Figure 1(c) shows Si surfaces after 400°C annealing. The erosion pattern (Al spikes) disappears in 1.2µm and 2.0µm holes. The shape of 0.7µm holes did not change, but that of 1.2µm and 2.0µm hole reverted to the initial shapes before deposition. The profile of the Al-Si interface was measured for 2.0µm holes by AFM and is shown in Fig 2. After deposition (a), the size of holes was larger than that before the deposition and the depth of the spike was



Fig. 1 SEM photographs of selectively deposited Al and Si surface after removal of Al and SiO2



Fig. 2 AFM profiles of eroded Si surface of 2.0µm contact hole

190nm. However, after annealing (b), the size was almost the same as that before deposition and the interface between Al and Si became extremely flat. The same result was obtained with 1.2 $\mu$ m holes. Table I shows the depth of eroded Si (x<sub>er</sub>), which was estimated from AFM measurement. Here, the depth was measured from the etched surface at contact-etching. In the 1.2 $\mu$ m and 2.0 $\mu$ m holes, x<sub>er</sub> after annealing was shallower than x<sub>er</sub> at spikes but deeper than x<sub>er</sub> at the flat part before annealing. x<sub>er</sub> in the 0.7 $\mu$ m hole became deeper with annealing, but was much shallower than x<sub>er</sub> in 1.2 $\mu$ m and 2.0 $\mu$ m holes. Tsubouchi et. al. reported that erosion-free and spike-free Al-Si direct contact was realized through selective deposition of single-crystal Al

Table I The depth of eroded Si  $(x_{er})$ , which was estimated from AFM measurement

		2.0µm contact hole	1.2µm contact hole	0.7µm contact hole	
as-deposited	flat part	15nm	10nm	12nm	
	spike	190nm	150nm		
after annealig at 400°C	flat part	100nm	70nm	39nm	

using DMAH.<sup>4)</sup> Our result is inconsistent with their result. Based on our results, the mechanism of the improvement of the Al-Si interface in the case of polycrystalline Al is considered as follows. Al spikes are



Fig. 3 Leakage current of 2.0µm n<sup>+</sup> contact

formed locally by dissolution of Si at the grain boundary of Al. During annealing at 400°C, Si in the grain boundary of Al is swept out and grows epitaxially into spike regions of the Si substrate.

## 3-2 Electrical properties of n+/p diode

Figure 3 shows junction leakage current of 2.0µm n+ contact holes at xi of 230nm. The deepest Al spike was formed in this case. After Al deposition (a), junction leakage current was found to increase from about 2V. However, after annealing at 400°C (b), the increase of junction leakage current was not found to 10V. This change may be due to the improvement of the interface. Contact resistance ( $\rho_c$ ) of 2.0µm contact holes was measured by the Kelvin method and is shown in Table II. With 400°C annealing,  $\rho_c$  at  $x_j$  of 230nm increases and is much larger than  $\rho_c$  of sputtered Al-1%Si, while  $\rho_c$  at x<sub>j</sub> of 330nm increases slightly but is the same as  $\rho_c$ of sputtered Al-1%Si. At the spikes, Si grows epitaxially with annealing, and there was the fear that this epitaxial Si induces increase of  $\rho_c$  but the above findings exclude this possibility. The impurity concentration at the eroded Si surface  $(n_s)$  depends on  $x_i$  and  $x_{er}$ , as shown in this table. The large increase of  $\rho_c$  at  $x_i$  of 230nm due to annealing is explained by the large decrease of ns.

Table II Contact resistance ( $\rho_c$ ) and impurity concentration ( $n_s$ ) of 2.0 $\mu$ m contact hole of as-deposited and after annealing at 400°C

		1월 1월 1413	junction depth ( simulated )				
		depth of	230nm		330nm		
		erodeu Sr	ρο	ns	ρο	ns	
CVD-Al	as-deposited	15 [nm]	<b>12.9</b> [Ω]	3.26x10 <sup>20</sup> [cm <sup>2</sup> ]	14.9 [Ω]	2.17x10 <sup>20</sup> [cm <sup>2</sup> ]	
	after annealing at 400°C	100 [nm]	7 <b>3.9</b> [Ω]	7.21x10 <sup>19</sup> [cm <sup>2</sup> ]	15.7 [Ω]	2.00x10 <sup>20</sup> [cm <sup>2</sup> ]	
sputtered - Al	as-deposited		2	3.26x10 <sup>20</sup> [cm <sup>2</sup> ]		2.17x10 <sup>20</sup> [cm <sup>2</sup> ]	
	after annealing at 400°C	—	16.8 [Ω]	3.26x10 <sup>20</sup> [cm <sup>2</sup> ]	<b>15.6</b> [Ω]	2.17x10 <sup>20</sup> [cm <sup>2</sup> ]	

### **§4** Conclusions

The interaction between Al deposited selectively by CVD and Si have been investigated. The structure of selectively deposited Al depends on the contact hole size. After deposition, Si was eroded uniformly by singlecrystalline Al and nonuniformly by polycrystalline Al. However, after annealing at 400°C, the interface between Al and Si was improved and became extremely flat. Low leakage current is obtained in the Al-Si direct contact after this annealing. The result of  $\rho_c$  measurement shows that epitaxially grown Si at the spikes, which gives the very flat Al-Si interface, does not influence  $\rho_c$ . These results indicate that the selective CVD Al has potential for use in the Al-Si direct contact.

### **References**

1) T. Amazawa and H. Nakamura: Extended Abstracts of the 18th Conference on Solid State Devices and Materials, Tokyo, 1986 (Business Center for Academic Societies Japan, Tokyo, 1986), p.755.

2)A. W. E. Chan and R. Hoffmann: J. Vac. Sci. & Techol. A9 (1991) 1569.

3)C. Sasaoka, Y. Kato, and A. Usui, Extended Abstracts of the 50th Autumn Meeting of the Jpn. Soc. Appl. Phys., Fukuoka, Sep., 1989, 29a-D-2 [in Japanese].

4)K. Tsubouchi, et. al., VLSI Symposium Technical Digest (1990)