Thermal Stability of an Interconnect of TiN/Cu/TiN Multilayered Structure

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The etching process for Cu interconnect with self-align deposition of a sidewall film has been developed. This sidewall film acts as oxidation barrier in a following process. Using this etching process, the Cu interconnect of a TiN/Cu/TiN multilayered structure in a submicron feature is formed. Resistivity for the Cu interconnects is about 2μΩ·cm, and it does not change on annealing up to 700°C. In the resulting Cu interconnect, a wedge-like void is not observed after annealing.

1. Introduction
Copper is the major candidate material of post-Al alloys in deep-submicron region, because of low resistivity and long electromigration lifetime. However, some problems on realization of the Cu interconnect have been reported, such as patterning, corrosion, and diffusion of Cu. To prevent diffusion of Cu into the Si substrate, we must use a multilayered structure; barrier metals are layered up and down sides of a Cu layer. Then the etching of such structure is important subject to obtain Cu interconnects with high reliability. In this work, we have developed a patterning process of a TiN/Cu/TiN multilayered interconnect, and have evaluated thermal stability of this interconnect concerning the resistivity and the structure.

2. Experimental
A multilayered film which is composed of TiN(0.1μm)/Cu(0.4μm)/TiN(0.1μm) was prepared on a thermally oxidized Si wafer by dc magnetron sputtering. A TiN layer was used as a barrier layer. A SiO2 film used as an etching mask was deposited on the multilayered film by plasma enhanced CVD. Etching was performed with a SiCl4/Cl2/N2 gas mixture, gas pressure of 20-35mTorr and a rf power of 500W using a magnetron reactive ion etching (RIE) system. In this system, a wafer in contact with a heat-block was controlled in the temperature range of 200-400°C. The wafer temperature was directly measured by a luminescent probe on the back side of a wafer.

3. Results and discussion
3.1 Etching Cu interconnect with self-aligned sidewall deposition
It is well known that Cu is mainly sublimed as (CuCl)3 above 150°C. Under our typical condition, etching of Cu was started at 220°C, and the etching rate was saturated above 300°C. Therefore, etching temperature was settled in 300°C to obtain a high etching rate and a good repeatability.

Side-etching of Cu patterns can be reduced with increasing N2 flow in a total gas flow. This fact is appreciated as a result of the thin protection film formed on the sidewall. It is expected that such protection film can be applied to self-aligned passivation to avoid oxidation of Cu during subsequent process. Therefore, to control the side-etching and the thickness of the self-aligned sidewall film, the effect of the number of each constituent atom, [N], [Si] and [Cl], in the introduced gas

Fig. 1 Dependence of thickness of the sidewall film on [Si]/[Cl].
mixture was investigated. A value of \([\text{N}]/[\text{Cl}]\) dominantly affects side-etching, and the \([\text{N}]/[\text{Cl}]\) ratio of more than 2 is necessary to prevent side-etching. As shown in Fig.1, thickness of the sidewall film is controlled by \([\text{Si}]/[\text{Cl}]\), and it is saturated when \([\text{Si}]/[\text{Cl}]\) is over 0.17.

On the basis of these results, etching of Cu is performed typically at 300°C and 35mTorr in a flow rate of \(\text{SiCl}_4/\text{Cl}_2/\text{N}_2\) of 20 /10 /120 sccm, which corresponds to \([\text{N}]/[\text{Cl}]=2.4\) and \([\text{Si}]/[\text{Cl}]=0.2\). On this etching condition, the etching rate of Cu and thickness of the sidewall film were 150nm/min and 70nm, respectively. Cross sectional view of the interconnect after etching is shown in Fig.2. According to AES analysis, the sidewall film is composed of \(\text{SiO}_x\) containing small amounts of impurities as shown in Table 1. Previous reports\(^3,4\) suggested such sidewall film had \(\text{SiN}\) like composition. However, on our work, content of nitrogen is less than 5 atomic\%. Chlorine, which causes corrosion of Cu, is contained less than 1 atomic\%. As-etched Cu line did not corrode after exposure to the atmosphere for 40 days after etching process. This fact differs from Al etching case. A little content of chlorine in the sidewall film is explained owing to vaporization of chloride, such as \(\text{TiCl}_x\) and \(\text{SiCl}_x\), in etching process. Because the wafer temperature of 300°C is high enough for these chlorides to vaporize from the sidewall film. Figure 3 shows the resistance changes \((R/R_0)\) of the Cu line with the sidewall film and a Cu film after annealing in air at various temperatures for 1 hour. Resistance of the Cu line shows no change up to 220°C, that is, the sidewall film of 70nm thick prevents Cu from oxidation up to this temperature. Therefore, the sidewall film acts as a barrier to prevent Cu from oxidation in the following NSG deposition process.

![Figure 2](image2.png)

*Fig.2 Cross sectional view of the interconnect after etching. Thickness of a sidewall film is about 70nm.*

![Figure 3](image3.png)

*Fig.3 Resistance change \((R/R_0)\) after annealing in air. The Cu line is 1.0 \(\mu\)m wide and 22nm long.*

### 3.2 Thermal stability of TiN/Cu/TiN interconnect

After etching process, the interconnect was covered with \(\text{SiN}(0.8\mu\text{m})/\text{NSG}(0.2\mu\text{m})\) as passivation layer (Fig.4) and sintered in \(\text{H}_2/\text{N}_2\) ambient at 400°C for 1 hour. After sintering, the resistivity estimated from line resistance was in the range of 2 - 3\(\mu\Omega\cdot\text{cm}.*

![Figure 4](image4.png)

*Fig.4 Cross sectional view of the interconnect after the whole process.*

Figure 5 shows resistivity of the Cu interconnect of 1.0\(\mu\text{m}\) wide and 22mm long after annealing at 450 - 800°C for 1 hour in vacuum. The resistivity does not change after annealing in the range of 400°C - 700°C. This thermal stability is revealed regardless of line-width up to 700°C as shown in Fig.6. The dependence of \(R/R_0\) on linewidth at 800°C is supposed to be not due to diffusion of impurities such as \(\text{Si}, \text{O}, \text{and Ti, because diffusion length of these impurities in Cu is much longer than 10}\mu\text{m at 800°C. This increase of resistivity is probably caused by void growth and grain growth of Cu.}

### Table 1 Composition of the sidewall film.

<table>
<thead>
<tr>
<th>(\text{atomic%})</th>
<th>Si</th>
<th>O</th>
<th>N</th>
<th>Cl</th>
<th>C</th>
<th>Cu</th>
</tr>
</thead>
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<td></td>
<td>59</td>
<td>22</td>
<td>3</td>
<td>1</td>
<td>10</td>
<td>5</td>
</tr>
</tbody>
</table>

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The overview of 4tm wide lines. (a) Cu line after 800°C annealing; (b) Al-Si line after 500°C annealing. A passivation layer and TiN barrier (for Cu line) were removed.

Figure 7 shows the overview of the Cu line and the Al-Si line after annealing. Sidewall of Cu line is smooth and no wedge-like void are observed after annealing up to 800°C. This fact is much different from Al-Si case, which is understood by the difference in an oxide formation energy between Cu(-73 kcal/g.molO2) and Al(-254 kcal/g.molO2) in comparison with that of Si(-196 kcal/g.molO2). In the interconnect of Al alloys, adhesion between Al alloy grain and SiO2, which covers the interconnect, is strong because of reduction of SiO2 by Al. Therefore, the void grows in the local area, such as grain boundary, and the void forms into wedge-like. In the Cu interconnect, adhesion between Cu and SiO2 is poor, because Cu does not reduce SiO2. Therefore, the void grows in an interface of SiOx/Cu uniformly, and the void does not form into wedge-like inducing the line failure5). The property of SiOx/Cu interface contributes the thermal stability of the Cu interconnect up to 700°C.

4. Conclusions
We have developed the etching process for Cu interconnect with self-align deposition of the sidewall film. This sidewall film acts as oxidation barrier in a following process. Using this process, the Cu interconnects of 0.8 - 10 µm wide is formed. Resistivity for the Cu interconnects is about 2 µΩ·cm, and is thermally stable up to 700°C. In addition, a wedge-like void is not observed in the Cu interconnect after annealing. Therefore, the developed Cu interconnect is advantageous in view of stress-induced migration lifetime, besides electromigration lifetime.

5. References