

Accelerated Electromigration Testing of Giant-Grain Copper Interconnects under Extremely Large Current Stress

T. Hoshi,¹⁾ H. Yamada,¹⁾ T. Takewaki,^{1),2)} T. Shibata,¹⁾ T. Ohmi,¹⁾ and T. Nitta³⁾

¹⁾Department of Electronic Engineering, Tohoku University,
Aza-Aoba, Aramaki, Aobaku, Sendai 980, Japan, TEL:022-224-2649, FAX:022-224-2549

²⁾Laboratory for Microelectronics, Research Institute of Electrical Communication,
Tohoku University, 2-1-1 Katahira, Aobaku, Sendai 980, Japan

³⁾Device Development Center, Hitachi Ltd. 2326 Imai-cho, Oume-shi, Tokyo 198, Japan

ABSTRACT

By using a newly-developed electromigration lifetest method under extremely large current stress, we have evaluated electromigration resistance of giant-grain copper interconnects. From the results of lifetests, we have demonstrated giant-grain Cu interconnects have much larger electromigration resistance than Al-alloy interconnects. Furthermore, we have discovered a new mode of electromigration failure occurring in Cu interconnects. Cu atoms move to the direction traversing the electron flow when an extremely large current stress condition is employed.

INTRODUCTION

The enhancement in the integration density and speed performance of ULSI circuits requires the miniaturization of transistors and interconnects as well as higher current driving capabilities for transistors. As a result, large currents must be conducted through long interconnections having small cross sections. Therefore the establishment of new metallization scheme which ensures high electromigration reliability as well as low electric resistance is extremely important. There has been much interest in Cu because of its high conductivity as well as high resistance to electromigration failures[1]. Recently, we have shown Giant-grain copper thin films having grain sizes as large as several hundred microns are ideal for use in high-speed ULSI interconnects. Such giant-grain Cu films were created by a low-energy ion bombardment process[2] and a subsequent thermal annealing. However, it has been very difficult so far to evaluate the reliability of Cu interconnects due to its extremely large electromigration resistance. It takes too much time to observe degradation in the test interconnect with conventional stress technique.

The purpose of this paper is to demonstrate their superior electromigration resistance, in particular under extremely large current stress, using a newly-developed accelerated testing method[3]. Of particular importance in evaluating the electromigration resistance of Cu interconnects is the employment of inert ambient, thus avoiding the copper oxidation during the test. As a result, we have shown that the giant-grain Cu interconnects exhibit more than one order of magnitude

larger resistance as compared to Al-Si-Cu interconnects. Furthermore, we have discovered a new mode of electromigration failure occurring in Cu interconnects when an extremely large current stress ($\geq 2.3 \times 10^7 \text{ A/cm}^2$) condition is employed.

EXPERIMENTAL

1 μm -thick Cu films were formed on SiO₂(100nm thick) by RF-DC coupled mode bias sputtering. Substrate bias voltages (Vs) of -80V was employed to create giant-grain copper films(100 μm) after thermal annealing, which was carried out in Ar ambient at 350°C for 6 hours. These Cu films were then patterned by wet etching to form test interconnects which were 4-5 μm in width and 80 μm in length. As a result, the Cu test interconnects having giant-grains have at most one or two grain boundaries within a sample. Electromigration test was carried out using the newly-developed accelerated lifetest method illustrated in Fig.1 both in cleanroom air and in N₂ ambient. The acceleration was achieved by large current stress (more than 10^7 A/cm^2) and high temperature stress (100-200°C) due to the self heating of the test interconnects by the stress current[4]. This measurement procedure consists of two major cycles: one is a resistivity measurement cycle in which the resistance of a test interconnect is monitored at room temperature and the other is current stress cycle in which the test interconnect is stressed by large current density at an elevated temperature. As a result, it has become possible for the first time to evaluate the electromigration resistance of giant-grain Cu

interconnects in a very short period of time. For comparative studies, Al-Si-Cu interconnects (900nm thick) were formed by conventional sputtering process and tested using the same method.

RESULTS AND DISCUSSION

The results of electromigration test carried out in N₂ ambient are shown in Fig. 2. The figure shows the Arrhenius plots of $\tau\rho J^2$, where τ is the measured electromigration lifetime and ρJ^2 is the stress power density applied to the test interconnects. Therefore, $\tau\rho J^2$ indicates the total power given to a unit volume of Cu before it shows a certain degradation due to electromigration, a quantity representing an intrinsic material property. It is clearly seen that Cu interconnects exhibit at least one order of magnitude larger electromigration resistance than Al-Si-Cu interconnects. The activation energy determined by Black's formula[5] for giant-grain copper interconnects is 0.80eV. During the lifetest of Al-Si-Cu interconnects, the reduction in the interconnect resistance was observed at the initial stage. This is interpreted as the annealing effect due to the Joule heating. Therefore the activation energy of Al-Si-Cu interconnects can not be determined from the data because the degradation by electromigration and annealing of defects are occurring simultaneously.

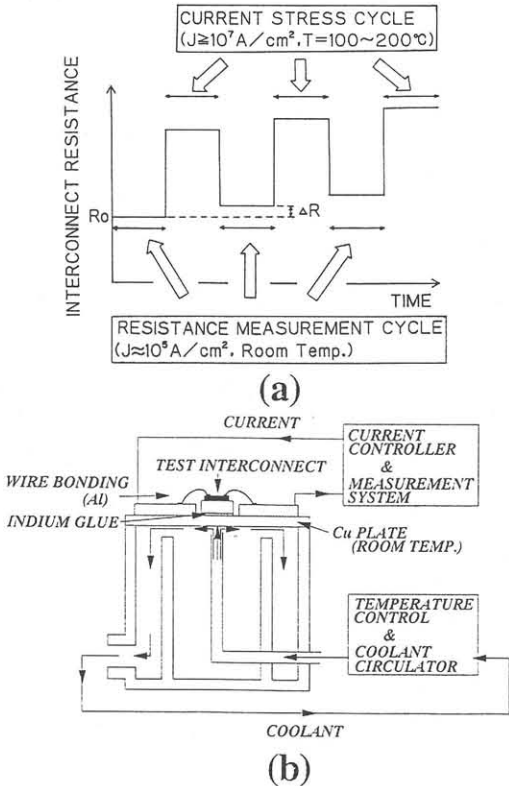


Figure 1 (a) Procedure of lifetest measurement. (b) A schematic of the measurement system used in the present work.

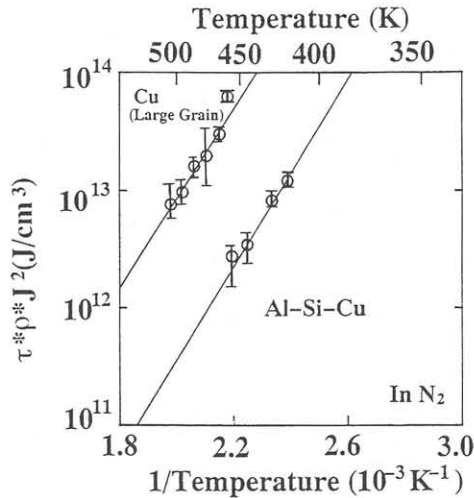
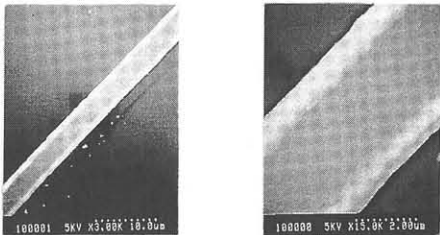


Figure 2 Results of lifetest in N₂ ambient for giant-grain Cu interconnects formed on SiO₂ by low-energy ion bombardment process and for Al-Si-Cu interconnects formed by conventional sputtering process.

BEFORE TEST



AFTER TEST

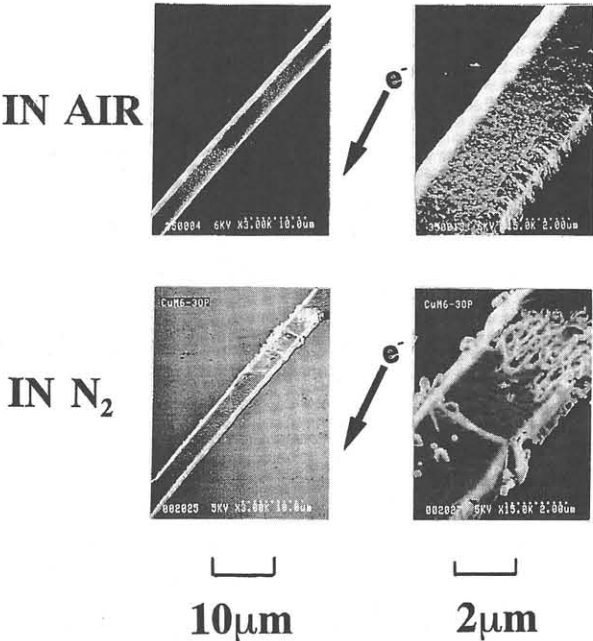


Figure 3 SEM micrographs of giant-grain copper interconnects before and after electromigration lifetest.

Figure 3 demonstrates the importance of testing ambient. After the lifestest in a cleanroom air, the surface roughness of Cu interconnect is seriously degraded by oxidation. However, in the case of the lifestest in N₂ ambient, the formation of voids and hillocks due to the electromigration are clearly visible at the upstream and downstream portions of the electron flow, respectively. The lifetime of Cu was about one order of magnitude larger in the N₂ ambient than in the air. Therefore the employment of a non-oxidizing ambient is quite essential for electromigration tests of Cu interconnects.

The results of electromigration lifestest for giant-grain copper interconnects evaluated both in cleanroom air and in N₂ ambient are summarized in Fig. 4. Cu interconnects evaluated in N₂ ambient exhibit one order of magnitude larger electromigration resistance than those evaluated in cleanroom air.

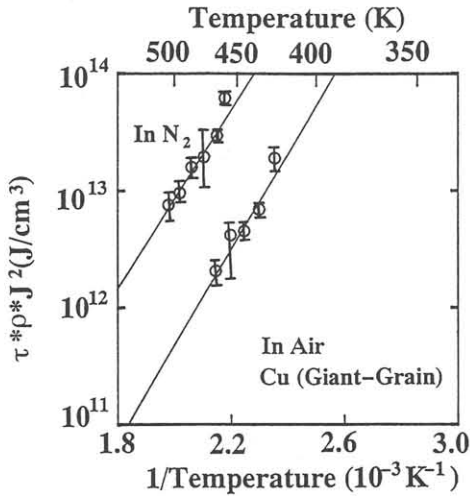


Figure 4 Arrhenius plots of $\tau\rho J^2$ for Giant-Grain Cu interconnects evaluated both in cleanroomair and in N₂ ambient.

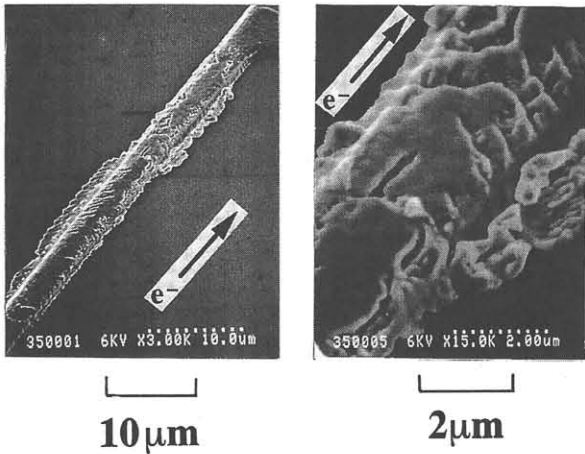


Figure 5 SEM micrographs of giant-grain Cu interconnects after lifestest under an extremely large stress current density($2.7\times10^7\text{A/cm}^2$).

Figure 5 shows the surface morphology of giant-grain Cu interconnects after lifestest under an extremely large stress current density($2.7\times10^7\text{A/cm}^2$). Unlike the degradation mode shown in Fig. 2 (see bottom two micrographs), it is interesting to observe that Cu atoms move to the direction traversing the electron flow as if they are avoiding the flood of electrons.

CONCLUSIONS

From the results of electromigration lifestests, it has been demonstrated that giant-grain Cu interconnects have much larger electromigration resistance than Al-alloy interconnect. Furthermore, we have discovered a new mode of electromigration failure occurring in Cu interconnects in which Cu atoms move to the direction traversing the electron flow. The giant-grain Cu interconnects are the most promising alternative to the Al-alloy interconnects for realizing ultra high speed ULSI's.

ACKNOWLEDGMENT

The majority of this work was carried out in Super Clean Room of Laboratory for Microelectronics, Research Institute of Electrical Communication, Tohoku University. The authors wish to thank Nikko Kyodo co., LTD, for providing the high-purity copper target.

[REFERENCES]

- [1] N. Awaya and Y. Arita, Dig. Tech. Papers, 1989 Symp. VLSI Technology, Kyoto, P.103.
- [2] T. Nitta, T. Ohmi, M. Otsuki, T. Takewaki, and T. Shibata, J.Electrochem. Soc., **139**, 922 (1992).
- [3] T. Nitta, T. Ohmi, T. Hoshi, S. Sakai, K. Sakaibara, S. Imai, and T. Ohmi, J.Electrochem. Soc., **140**, 1131 (1993).
- [4] B. J. Root and T. Turner, Proceeding of the 23rd annual Reliability Physics Symposium, p100, 1985.
- [5] J. R. Black, IEEE Trans. Electron Devices, ED-16, 338(1969).