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Impact of Dopant-Redistribution at $TiSi_2$/Si Interface and a Doubly-S/D-Ion-Implanted-SALICIDE Structure for Subhalfmicron CMOS

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It is concluded that the decrease of impurity concentration at the $TiSi_2$/Si interface due to silicidation significantly degrades device performances with a shallow junction required for subhalfmicron CMOS. It is verified for the first time that this degradation is due to dopant redistribution from Si to $TiSi_2$ during a post silicidation anneal, by evaluation of the contact resistance at the $TiSi_2$/Si interface and analysis of impurity concentration by means of PC-SIMS and a 2-dimentional process simulation including a SALICIDE process. In order to overcome the dopant redistribution effect, a novel SALICIDE process denoted as "DIS" (Doubly source/drain Ion implanted SALICIDE) is proposed and confirmed to be applicable for subhalfmicron CMOS.

1.Introduction

In a subhalfmicron MOSFET, a source/drain junction depth approaches to 0.1μm. Consequently, source/drain resistance increases to restrict a drivability of MOSFET. One of the attractive technology to reduce this source/drain resistance is a SALICIDE (Self-Aligned-Silicide) process. The SALICIDE process has another benefit to replace a silicon/metal contact of high resistivity to a silicide/metal contact of low resistivity.

However, in applying a SALICIDE process to a 0.1μm depth shallow junction, investigation of the impurity behaviour in silicide/silicon system is necessary. A shallow junction has a sharp profile of impurity concentration in vertical direction, with a peak at a surface. Silicidation in such a shallow junction induces a consumption of high impurity region and locates the silicide/silicon interface in the region of low impurity concentration. Therefore, the shift of impurity concentration due to redistribution at this low concentration interface may significantly enhance the degradation of a silicide/silicon interface in a shallow junction, as illustrated in Fig.1.

In this study, it is clearly verified that the dopant redistribution from Si to $TiSi_2$ at $TiSi_2$/Si interface during a post silicidation anneal significantly degrades the I-V characteristics of the subhalfmicron MOSFET. The result that the post silicidation anneal induces dopant redistribution is verified by evaluation of the interface resistance with Lynch's method[1] and analysis of impurity concentration by means of PC-SIMS and a 2-dimentional process simulation including a SALICIDE process.[2] Furthermore, to overcome the dopant redistribution effect, a novel SALICIDE process denoted as "DIS" (Doubly source/drain Ion implanted SALICIDE) is proposed and confirmed to be applicable for subhalfmicron CMOS.

2.Investigation of Dopant Redistribution Effect on a Shallow Junction

A. Experimental

PMOSFETs of junction depth ranging 0.1μm to 0.2μm, and of interface boron concentration ranging approximately 1E18 cm^{-3} to 1E20cm^{-3} are fabricated. The junction depth of source/drain and the boron concentration at the interface are varied by implantation dose of BF_2^+ ions and temperature of the sequential anneal to diffuse those ions. Approximately 70nm thickness $TiSi_2$ layer is formed on the source/drain region, by 40nm thickness Ti film deposition and sequential 2-step RTA (Rapid Thermal Anneal). The post silicidation anneal is applied with furnace at temperature ranging 850°C to 900°C, after the interlayer oxide is deposited.

The contact resistance of the $TiSi_2$/Si interface is evaluated by Lynch's method, which is a modified Kelvin's method including a MOSFET structure.[1] The interface resistance can be evaluated by arranging a current to pass through under a gate electrode, where silicidation is not applied.

In order to evaluate the boron concentration underneath the $TiSi_2$ layer precisely, PC-SIMS (Polysilicon Encapsulation SIMS) method is applied.[3] After the $TiSi_2$ layer is removed in HF solution, samples are dipped in $NH_4OH/H_2O_2/H_2O$ solution to exclude the signal from TiB, which is agglomerated at $TiSi_2$/Si interface.[4]

Impurity behaviour in $TiSi_2$/Si interface is investigated using the 2-dimentional process simulator, which is newly developed to study the SALICIDE process.[2] In this process simulator, diffusion of impurity in $TiSi_2$ and segregation of impurity at $TiSi_2$/Si interface are treated for the first time. Displacement of the interface during silicidation is also treated.

B. Results

I_{DS}-V_{DS} curve of MOSFETs with different post silicidation anneal temperatures are shown in Fig.2. Obviously, the post silicidation anneal degrades the I-V characteristics of MOSFET in linear region. I-V characteristics of the $TiSi_2$/Si interface of the same samples evaluated by Lynch's method are shown in Fig.3. This result indicates a barrier formation at the $TiSi_2$/Si interface after post silicidation anneal. The degradation in the I-V characteristics of MOSFET is explained by this barrier formation effect. These results suggest the decrease of impurity concentration at the $TiSi_2$/Si interface due to post silicidation anneal.

To verify the decrease of impurity concentration at the $TiSi_2$/Si interface due to the post silicidation anneal, impurity concentration underneath the $TiSi_2$ layer is evaluated by PC-SIMS analysis. Boron profile at the $TiSi_2$/Si interface before and after post silicidation anneal are shown in Fig.4. Significant decrease of boron concentration at the $TiSi_2$/Si interface after post silicidation anneal is verified.

To investigate the mechanism of decrease of boron concentration underneath $TiSi_2$ during post silicidation anneal, impurity behaviour of $TiSi_2$/Si system is analyzed by 2-dimentional process simulator. In Fig.5, the shift of boron profile due to post silicidation anneal is shown in both vertical and lateral direction. It indicates a significant decrease of boron concentration at the Si side of the interface, and complementary increase of boron concentration at the $TiSi_2$ side of the interface which is due to segregation effect at $TiSi_2$/Si interface.[5] This result is coincident with that of PC-SIMS analysis. From these results, it is verified that the post silicidation anneal induces the redistribution of boron from Si to $TiSi_2$ and a barrier formation at $TiSi_2$/Si interface, and as a result, the I-V characteristics of MOSFET is degraded.

In order to estimate the minimum impurity concentration at the $TiSi_2$/Si interface which is required to avoid a barrier formation, the relation between the interface concentration and the interface resistance is investigated. In Fig.6, the interface resistance after post silicidation anneal is plotted as a function of interface concentration of both after silicidation and after post silicidation anneal. Extreme increase in contact resistance indicates a increase of the barrier height at the $TiSi_2$/Si interface due to dopant redistribution. To avoid a barrier formation, approximately $3E19cm^{-3}$ of boron concentration at the interface is required after post silicidation anneal. After silicidation anneal, this value corresponds to $6E19cm^{-3}$. This value is extremely high in comparison with a 0.1μm depth shallow junction. Therefore, it is concluded that the conventional SALICIDE process is not applicable to a 0.1μm depth shallow junction due to dopant redistribution effect at the $TiSi_2$/Si interface.

3.Application of "DIS" Process to Subhalfmicron CMOS

In order to avoid a barrier formation at the $TiSi_2$/Si interface with a 0.1μm depth junction, it is required to supplement impurity at the silicide/silicon interface. The purpose of "DIS" (Doubly source/drain Ion implanted SALICIDE) process is to supplement impurity at $TiSi_2$/Si interface. The cross sectional structure of "DIS" is illustrated in Fig.6. After conventional source/drain is fabricated, a sidewall is formed and a SALICIDE structure is composed, sequentially the additional source/drain implantation is introduced to supplement impurity at the $TiSi_2$/Si interface. This additional implantation has no influence on short channel effect because the junction depth at the gate edge is determined by the conventional implantation.

I_{DS}-V_{DS} curves with and without "DIS" are shown in Fig.7. By applying "DIS", degradation of the I-V characteristics at linear region is improved. From this result, "DIS" process is effective to supplement impurity at the $TiSi_2$/Si interface.

To investigate the behaviour of boron in "DIS" process, the boron concentration after post silicidation anneal is obtained by simulation. Results of with and without "DIS" process is shown in Fig.8. Although redistribution of boron from Si to $TiSi_2$ due to segregation effect is found in "DIS" process, the concentration of boron underneath the $TiSi_2$ is sufficiently high compared with the conventional SALICIDE process. Therefore, the dopant redistribution effect does not affect on the I-V characteristics of MOSFET with "DIS".

To verify the another advantage of "DIS" process, junction leakage current is also evaluated in comparison with the conventional SALICIDE process. It is shown in Fig.9. In "DIS" process the junction leakage current is sufficiently suppressed compared with the conventional SALICIDE process. The suppression of junction leakage current by applying "DIS" process is caused by the sufficient distance between the $TiSi_2$/Si interface and the junction plain due to restriction of dopant redistribution.

4. Conclusion

By investigation of the $TiSi_2$/Si interface by Lynch's method, PC-SIMS analysis and newly developed process simulation, it is concluded that in a conventional SALICIDE process dopant redistribution from Si to $TiSi_2$ during a post silicidation anneal induces an interface barrier, a significant degradation of the I-V characteristics of MOSFET and junction leakage current.

In a 0.1μm depth shallow junction, where the region of high impurity concentration is consumed by silicide, the dopant redistribution at the silicide/silicon interface significantly enhances to lower the impurity concentration at this interface. Therefore the conventional SALICIDE process is not applicable to a 0.1μm depth shallow junction required for subhalfmicron CMOS.

To improve the dopant redistribution induced degradation, a novel SALICIDE process denoted as "DIS" is proposed and confirmed to be applicable to subhalfmicron CMOS.

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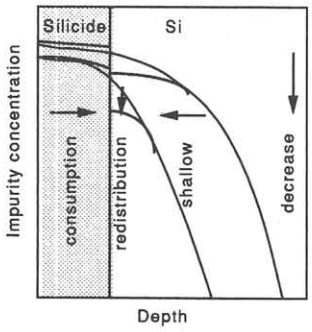


Fig.1 Degradation of the silicide/silicon interface in shallow junction

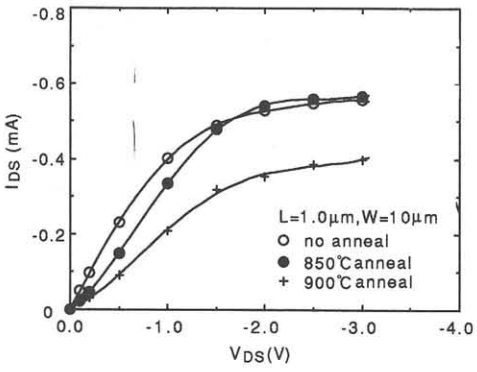


Fig.2 Dependence of the I-V characteristics of MOSFET on the post silicidation anneal

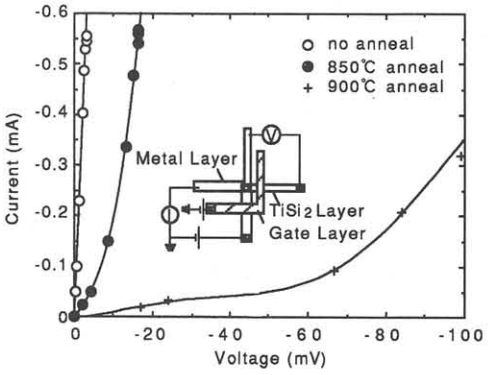
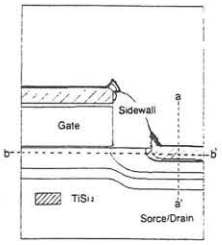
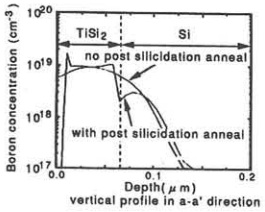


Fig.3 I-V characteristics of the $TiSi_2$/Si interface : Dependence on the post silicidation anneal





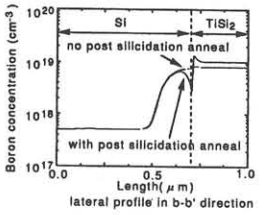


Fig.4 Boron profile of SALICIDE structure obtained by simulation

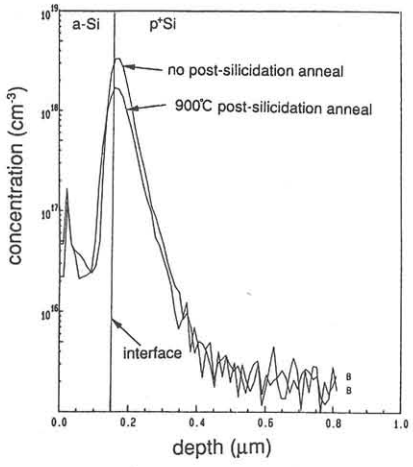


Fig.5 Boron profile underneath the $TiSi_2$/Si interface obtained by PC-SIMS analysis

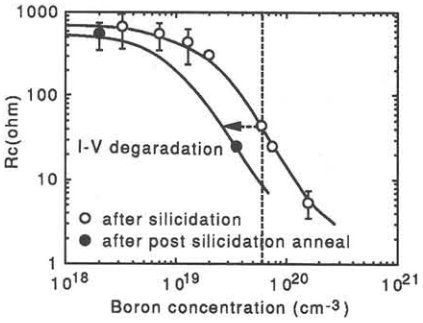


Fig.6 Dependence of the contact resistance on the boron concentration at the $TiSi_2$/Si interface : Contact resistance is plotted for both the concentration after silicidation and that of after post silicidation anneal.

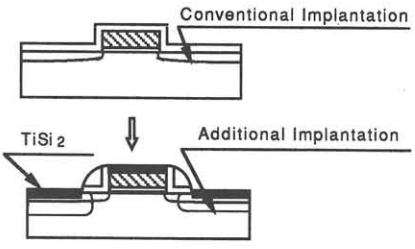


Fig.7 Cross section of "DIS" : Doubly source/drain Ion implanted SALICIDE

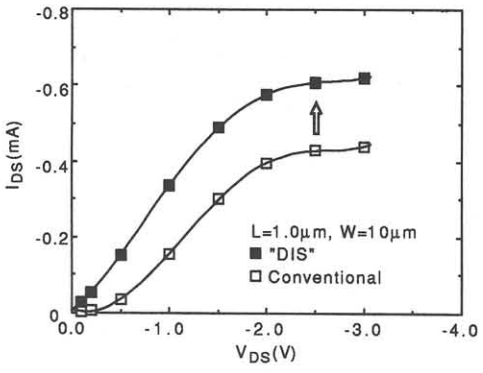


Fig.8 I-V characteristics of MOSFET : Comparison between "DIS" and conventional SALICIDE

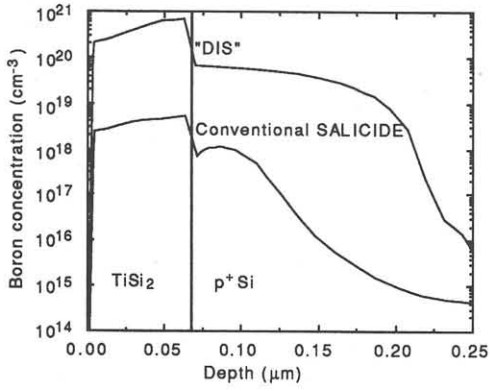


Fig. 9 Vertical profile of boron in $TiSi_2$/p⁺Si structure : Comparison between "DIS" and conventional SALICIDE

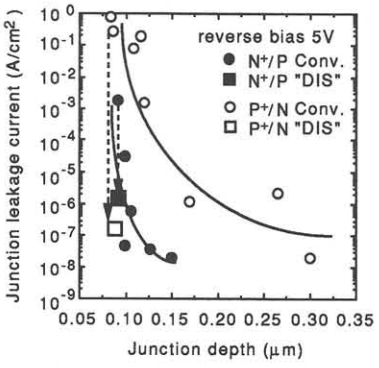


Fig.10 Dependence of junction leakage current on junction depth with conventional SALICIDE and Effect of "DIS" on junction leakage current