Extended Abstracts of the 1993 International Conference on Solid State Devices and Materials, Makuhari, 1993, pp. 567-569

A Low Parasitic Capacitance Scheme by Thermally Stable Titanium Silicide Technology for High Speed CMOS

Takehito Yoshida, Shinichi Ogawa, Akio Miyajima, and Kousaku Yano
Semiconductor Research Center, Matsushita Electric Industrial Co., Ltd.,
Moriguchi, Osaka 570, Japan

This paper presents titanium silicided junctions by a dopant drive-out process from elevated source/drain (S/D) structures combined with titanium silicide local interconnects, which reduce not only the S/D areas but also junction capacitance in advanced CMOS fabrication. The local interconnects which extend over field oxides are directly connected to the lining for the whole S/D regions. The titanium silicide of the local interconnects is formed from a reaction of an amorphous (a)-Si/Ti bilayer. A low oxygen content process with boron (B) doping using an optimized implantation energy realizes a thermally stable titanium silicide with reduced Ti-B compound formation. The delay time per stage of the MOSFETs with these local interconnects is about 18% faster than that of conventional contact structure devices.

1. Introduction

In most previous titanium silicidation methods, the advantages of a low parasitic resistance have been emphasized. Titanium silicide local interconnect technology is effective in reducing the parasitic junction capacitance as well as the parasitic resistance. For example, HPSAC is well known as such a local interconnect structure [1]. However, there have been no reports which clearly describe the effects on submicron circuit performance of parasitic capacitance reduced by the local interconnect scheme .

In this study, in order that we appreciate the relationship between S/D area shrinkage and high speed performance, a dopant drive-out process from elevated S/D, combined with the titanium silicide local interconnets, is adopted to retard lateral redistribution of B. A low oxygen content process is developed to realize thermal stability of the titanium silicide at 850-900 °C, which is necessary in the dopant drive-out process. Furthermore, B doping by optimized implantation energy is introduced for suppression of Ti-B compound formation [2].

2. Sample Preparation

Figure 1 shows the elevated S/D MOSFET structure with the titanium silicide local interconnects. After the formation of n^+poly-Si gate patterns, which was completely encapsulated by CVD-SiO_2, an a-Si/Ti bilayer was sputter deposited. The a-Si film in the bilayer was dry-etched off into the local interconnects and the S/D lining patterns. The nominal composition (X: TiSix) of the as-deposited a-Si/Ti bilayer was determined to be near stoichiometric for the disilicide (X=2.0). Silicidation was carried out by a rapid thermal annealing (825 °C). The thickness of the formed titanium silicide was 85 nm, and its sheet resistance was 1.85 Ω/sq.. Dopants (As^+, B^+) were implanted into the titanium silicide layers which covered whole S/D regions as linings. Two conditions of the dopant activation annealing were carried out in a conventional furnace. The first condition was at 900 °C for 60 min for 1.0 μm gate length (gate sidewall: 0.23 μm) MOSFETs. The second condition was at 850 °C for 60 min for 0.7 μm gate length (gate sidewall: 0.18 μm) MOSFETs. In the structure by this silicidation process, great portion of the titanium silicide layer was formed above the initial Si surface, so it is called an elevated S/D structure.

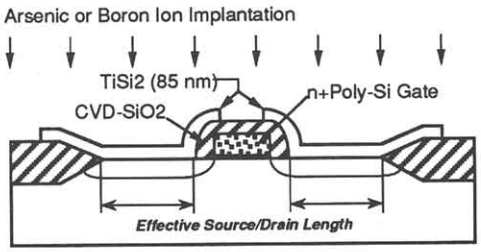

Fig. 1: Cross-sectional structure of elevated S/D MOSFET with titanium silicide local interconnects.

3. Results and Discussion

To prevent morphological degradation (agglomeration) in the titanium silicide local interconnects during annealing at 900 °C for 60 min, we adopted sputter etch cleaning and sputter-deposition of a-Si so that the maximum oxygen concentration at the

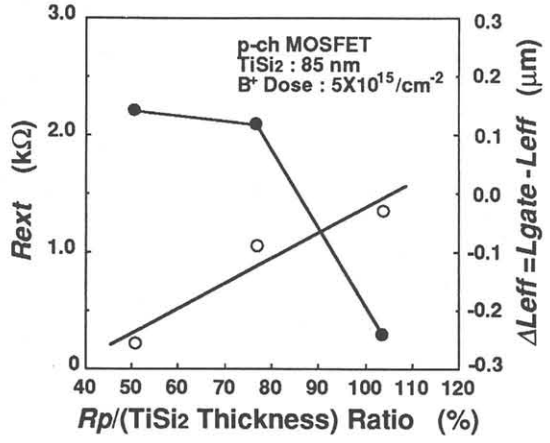

Fig. 2: Effective channel reduction (*ΔLeff*) and external resistance (*Rext*) as a function of B^+ projected ranges normalized by thickness of titanium silicide layer (Rp^n), in p-channel MOSFETs of elevated S/D with titanium silicide local interconnects.

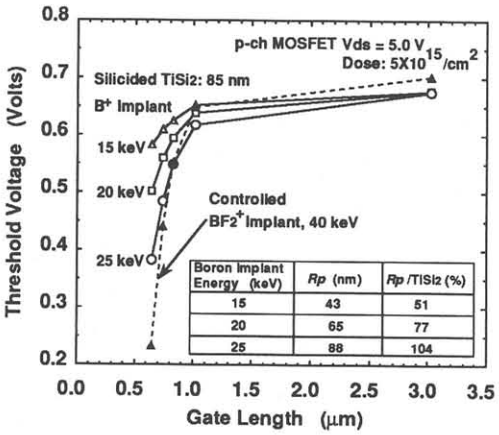

Fig. 3: Saturation threshold voltage of p-channel MOSFETs of elevated S/D with titanium silicide local interconnects.

as-deposited Ti/Si-substrate interface was less than $1X10^{20}cm^{-3}$ [3]. We believe that thermal stability against the 900 °C-60 min annealing allows us to use conventional furnace annealing for dopant activation with a large process margin.

To eliminate the Ti-B compound formation and consequent lowering of carrier concentration at the (titanium silicide)/Si interface, which would cause a very high series resistance, the B^+ implantation energies for the S/D regions were investigated under a constant dose of $5X10^{15}cm^{-2}$. In this experiment, the 1.0 μm gate length MOSFETs annealed at 900 °C for 60 min were used. Figure 2 shows the effective channel reduction (*ΔLeff*) and external resistance (*Rext*) [4] as a function of the B^+ projected range normalized by the titanium silicide thickness (Rp^n) in the p-channel MOSFETs. The *Rext* decreases rapidly for Rp^n greater than 80%. Even though the *Rp* of the B^+ was located at the (titanium silicide)/Si interface, the *ΔLeff* was kept near zero. This means that the lateral redistribution of B under the gate oxide did not occur even after the 900 °C-60 min annealing, when the gate sidewall width was 0.23 μm. When the *Rp* was located at the center of the titanium silicide layers ($Rp^n \approx 50\%$), the greater portion of B in the titanium silicide layers (estimated to be 81% of the total dosage) likely formed Ti-B compounds after the 850-900 °C activation annealing. When the *Rp* was located at the silicide/Si interface (Fig. 2: $Rp^n \approx 104\%$), 53% of the total dosage was in the Si substrate. Therefore this portion of the dosage could contribute to form carrieration, although the remaining dosage reacted with the titanium silicide and formed Ti-B compounds. Figure 3 shows the threshold voltage (*Vth*) as a function of gate length, compared with controlled devices (w/o the silicidation process, p^+ doping was performed by $BF2^+$ implantation at an energy of 40 keV). The MOSFETs with the elevated S/D structure had high resistance to *Vth* lowering. This result is consistent with the data of *ΔLeff* (Fig. 2). In this process, the geometrical advantage of the elevated S/D structure and a reduction of diffusant B in the Si substrate indeed contribute to the retarded lateral B redistribution.

The 0.7 μm gate length MOSFETs annealed at 850 °C for 60 min were evaluated. Figure 4 shows the *Ids-Vds* characteristics of the MOSFETs for the elevated S/D structure. The *Rp* of the implanted B^+ was located at the (titanium silicide)/Si interface. Both n-channel and

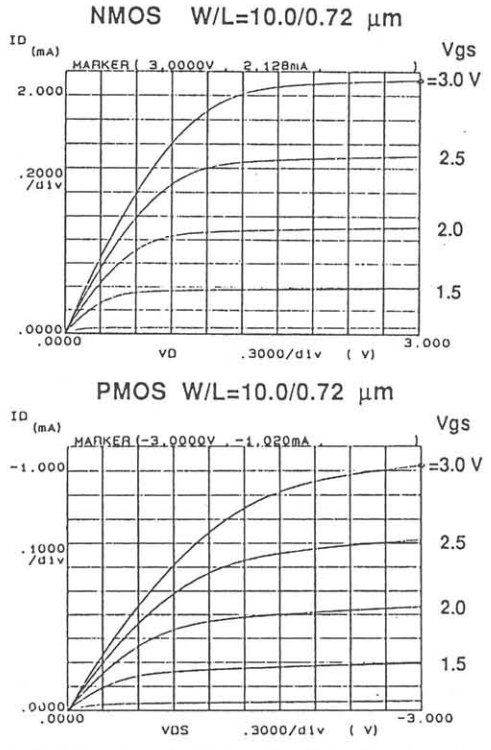

Fig. 4: *Ids-Vds* characteristics of optimized p-channel MOSFETs of elevated S/D with titanium silicide local interconnects.

p-channel MOSFETs normally operated. The pattern layout of the CMOS ring oscillator using the titanium silicide local interconnects is shown in Fig. 5. Figure 6 shows the delay time per stage (τ) as a function of the effective S/D length (cf. Fig. 1). In the local interconnect scheme, the effective S/D length can be reduced to 0.55 μm, because the contacts are formed on the isolation oxide. The τ decreased with reducing effective S/D length. Dependence of the measured junction capacitance on the effective S/D length is shown in Fig. 7. The reduction of total capacitance was almost equivalent to the τ reduction. The τ of the local interconnect scheme was about 18% faster than that of conventional contact structure devices for which the effective S/D length was estimated to be 1.5 μm in 3.0 V operation.

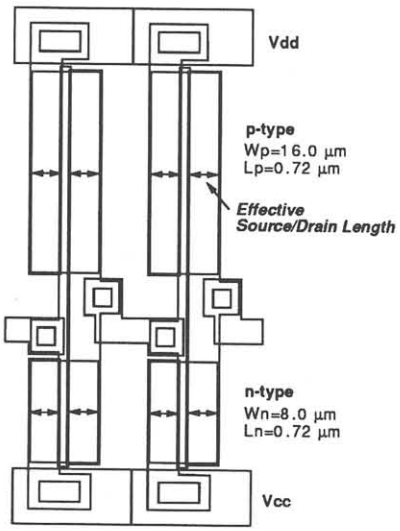

Fig. 5: Pattern layout of CMOS ring oscillator (F/O=1) using titanium silicide local interconnects.

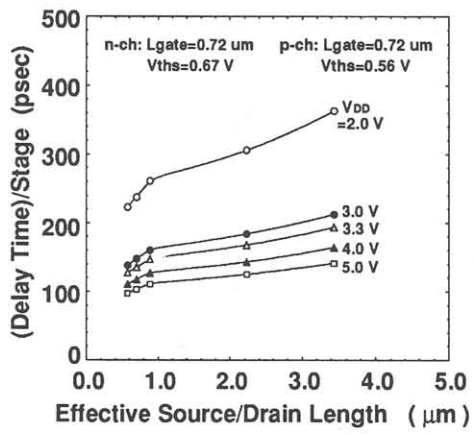

Fig. 6: Delay time per stage of submicron CMOS with titanium silicide local interconnects as a function of effective S/D length.

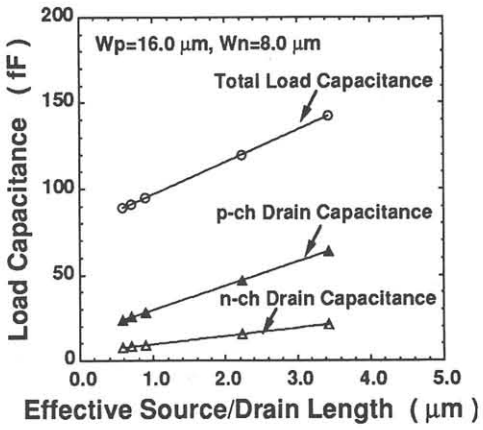

Fig. 7: Dependence of S/D junction and total load capacitance on effective S/D length with titanium silicide local inter-connects.

4. Conclusion

A low parasitic capacitance scheme using a dopant drive-out process from an elevated S/D structure and titanium silicide local interconnects has been realized by the thermally stable silicidation with the reduced Ti-B compound formation. It has been demonstrated that this method has an impact on high speed and low power submicron CMOS devices.

5. Acknowledgements

The authors would like to express their thanks to A. Shinohara for his helpful discussion. We also wish to acknowledge S. Akiyama, N. Nomura and M. Inoue for their continuous encouragement throughout this work.

6. References

[1] S. S. Wong, D. C. Chen, P. Merchant, T. R. Cass, J. Amano, and K-Y. Chiu, IEEE Trans. on Electron Devices ED-34, 587 (1987).
[2] K. Maex, G. Ghosh, L. Delaey, V. Probst, P. Lippens, S. Van den Hove, and R. DeKeersmaecker, J. Mater. Res. 4, 1209 (1989).
[3] T. Yoshida and S. Ogawa, J. Vac. Sci. & Technol. B 9, 1950 (1991).
[4] G. J. Hu, C. Chang, and Y-T Chia, IEEE Trans. on Electron Devices ED-34, 2469 (1987).