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Silicon Wafer Orientation Dependence of MOS Device Reliability

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The reliability of very thin gate oxides is studied using Si(100) and Si(111) wafers. When the oxide on Si(111) gets thicker, the Si-SiO_2 interface microroughness increases and consequently the dielectric breakdown characteristics are degraded. The oxide films on Si(111) are inferior to those on Si(100) in the reliability under the same level of the Si-SiO_2 interface microroughness, and the oxide film structure on Si(111) is different from those on Si(100). Oxide quality is determined by silicon wafer surface orientation.

1. INTRODUCTION

The perfect control of wafer surface microroughness is an important factor for the fabrication of MOS devices, because the surface microroughness causes the degradation of MOS device performances[1,2]. The degradation of dielectric breakdown characteristics is caused by the concentration of electric field in parts of projections. It is uncertain whether the degradation of MOS device performances is caused by only geometric configuration or other effects of the surface microroughness. The surface microroughness mainly increases in APM solution having high NH_4OH concentration during chemical cleaning. Si(100) surface is etched faster than Si(111) surface, and consequently Si(111) surface partly appears on Si(100) wafer. Because Si(111) surface is stabile in chemical solution. This is the reason for the increase in surface microroughness. In other words, a Si(100) wafer with large surface microroughness have two kinds of surface orientation, Si(100) and Si(111). So two kinds of oxides, oxide on Si(100) surface and oxide on Si(111) surface, are formed and mixed. Therefore, it is necessary to compare oxide quality on Si(111) with that on Si(100). The studies of producing an atomically flat Si(111) surface are reported[3,4], but the reliability of very thin oxide on Si(111) wafer have not been revealed sufficiently yet. The purpose of this paper is to clarify the effect of wafer orientation on very thin oxide reliability. As a result, we have showed that silicon wafer orientation dominates the reliability and the structure of oxide.

2. EXPERIMENTAL

The oxidation was carried out in the ultraclean environment characterized by extremely low metal and airborne impurity concentrations to reveal the effect of Si wafer orientation only[5]. MOS devices were fabricated on the wafer with the field oxide of non-doped silicate glass(NSG) having 500nm oxide thickness(without field oxide) and the wafer with the field oxide formed by wet oxidation at 1000°C for 4hours(with field oxide). The average Si-SiO_2 interface microroughness(Ra) was measured with Atomic Force Microscopy(AFM), where the height accuracy is the order of 0.1nm[6].

3. RESULT AND DISCUSSION

Figure 1 shows the relationship between Si-SiO_2 interface microroughness and oxide thickness. The dry oxidation was employed to form the oxide with thickness below 100nm, while wet oxidation was employed to form the oxide thickness of 100nm or thicker. The Si-SiO_2 interface microroughness was measured by AFM after removing the oxide with advanced BHF[7]. The Si-SiO_2 interface smoothness for Si(111) with oxides less than 10nm is the same as that for Si(100). The Si-SiO_2 interface microroughness on Si(111) increases as the oxide gets thicker. These results indicate that the behavior of Si-SiO_2 interface microroughness strongly depends on silicon wafer orientation.

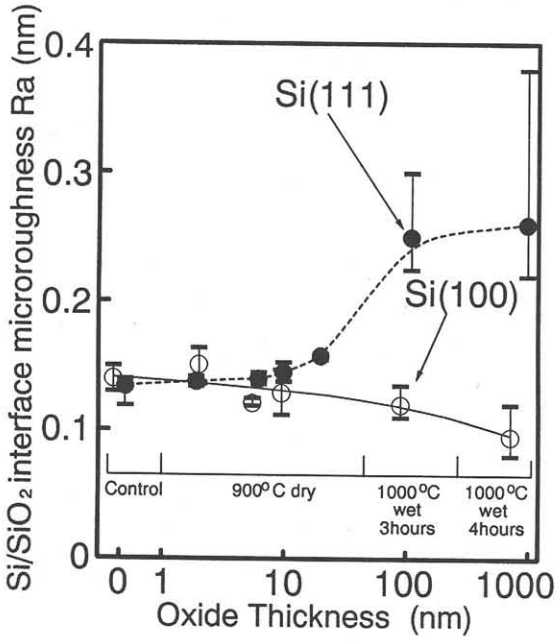

Figure 1. The relationship between Si–SiO_2 interface microroughness and oxide thickness.

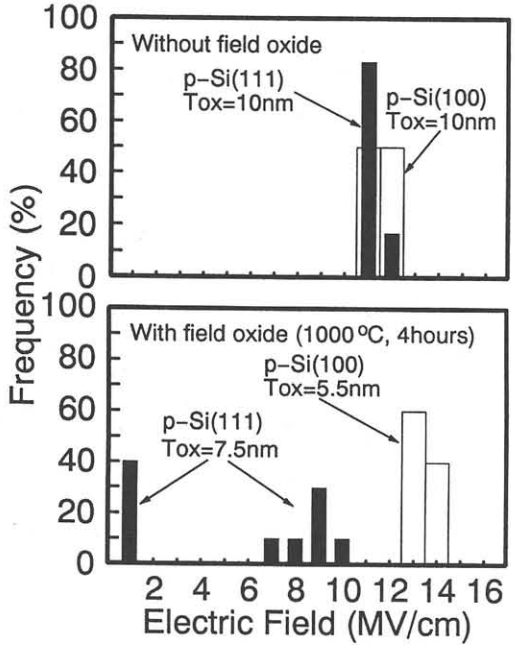

Figure 2. The dielectric breakdown histogram for Si(100) and Si(111).

Figure 2 shows the dielectric breakdown characteristics of MOS diodes (n^+–polycrystalline $Si/SiO_2/p$–Si) for Si(100) and Si(111) under negatively biased metal electrodes, where these MOS diodes are fabricated on wafer "without field oxide" (a) and wafer "with field oxide" (b). The gate oxides were formed by dry oxidation at 900°C. The device area is $1\times10^{-4}cm^2$ and the criteria for dielectric breakdown is a current of $1\times10^{-4}A$. In the case of (a), low field breakdown event is never observed on Si(100) and Si(111). While in the case of (b), many low field breakdown events are

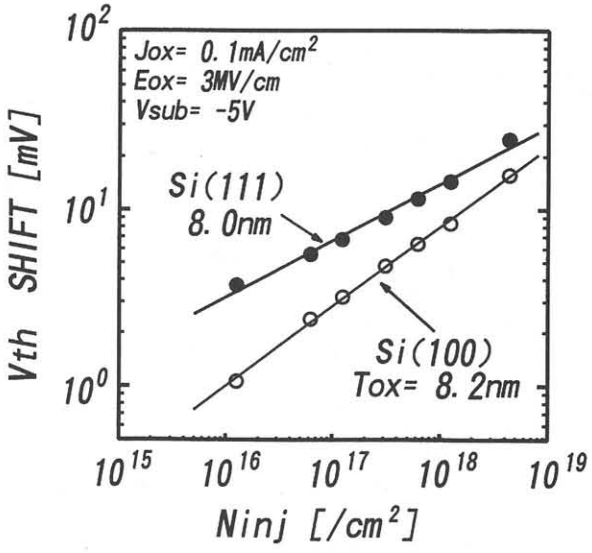

Figure 3. The threshold voltage shift of n–MOSFET as a function of the number of injected electrons.

observed on Si(111). It is considered that the increase in Si–SiO_2 interface microroughness causes low field breakdown, and breakdown field events for oxides on Si(111) and Si(100) are maintained at high fields under the small Si–SiO_2 interface microroughness.

Figure 3 shows the threshold voltage shift of n–MOSFET as a function of the number of injected electrons. The hot electrons are injected from silicon substrate into gate oxide, using pn junction fabricated near the measured devices[8,9]. During hot electrons injection, the current density into gate oxide is $0.1mA/cm^2$, the oxide field is 5MV/cm and the substrate bias is –5V. These n–MOSFETs were fabricated on wafer "without field oxide" in order to keep the same level in Si–SiO_2 interface microroughness of Si(111) as Si(100). The shift for Si(100) is smaller than that for Si(111). This result indicates that the oxide on Si(111) easily generates negative fixed oxide charges and electron traps during electrons injection compared with that on Si(100).

Figure 4 shows the etching depth of oxide films as a function of etching time. The etching of oxide films is done at 23°C by using BHF solution having low etching rate. The oxide thicknesses are measured by ellipsometry. The etching rate for the oxide film on Si(111) is larger than that on Si(100). This result suggests that the structure of the oxide formed on Si(111) is different from that on Si(100).

Figure 5 shows that the Si_{2P} XPS spectra of 27nm and 930nm oxides for Si(100) and Si(111). For 930nm oxides, the oxide was etched off partially and X-ray was irradiated at the boundary between silicon and SiO_2. This was done because the maximum oxide

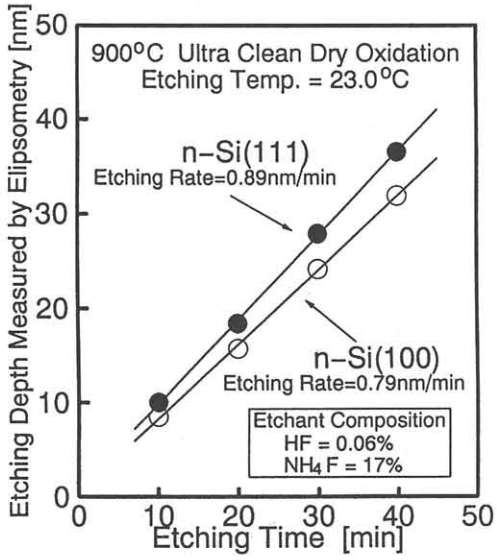

Figure 4. Etching depth of oxide films as a function of etching time.

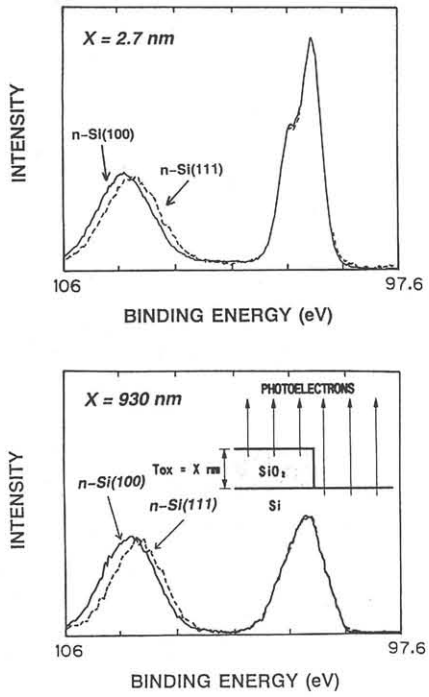

Figure 5. The Si_{2p} XPS spectra for the oxides on Si(100) and Si(111).

thickness that XPS signals of both SiO_2 and substrate silicon can be observed is 14nm. The binding energy of oxide peak for Si(111) is lower about 0.20eV than that for Si(100), and the binding energy difference doesn't depend on the oxide thickness. It is considered that the oxides on Si(111) are different from those on Si(100) in the structure of both SiO_2 bulk and Si-SiO_2 interface.

4. CONCLUSION

It is found that the quality of very thin oxides strongly depends on silicon wafer surface orientation. The oxide on Si(111) is inferior to that on Si(100) in reliability, and the structure of oxide on Si(111) is different from that on Si(100). The increase of the surface microroughness partly causes the appearance of Si(111) surface on a Si(100) wafer and causes the formation of the oxide mixed both the oxide on Si(111) and the oxide on Si(100), and consequently makes the reliability of the oxide degenerate. Therefore, the production of the wafers having accurate Si(100) orientation never having off-angle and atomically flat surface is extremely important for the fabrication of highly reliable MOS devices.

5. ACKNOWLEDGEMENT

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6. REFERENCES

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