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Highly Reliable Oxynitride Gate Dielectrics for Dual Gate CMOS Applications

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Several oxynitride gate dielectrics (NH_3-nitrided, reoxidized NH_3-nitrided, N_2-annealed NH_3-nitrided and N_2O grown oxides) are investigated and compared for use in p^+-polysilicon gate MOS devices. The comparison is based on flatband voltage shift as well as decrease in inversion capacitance. Due to the inadequacy of N_2O and NH_3-based gate dielectrics to achieve excellent hot-carrier reliability and excellent boron stopping potential simultaneously, a novel technique involving processing in both N_2O and NH_3 is developed, essential for aggressively scaled dual gate CMOS devices.

1. INTRODUCTION

Oxynitride gate dielectrics have received a considerable attention as a substitute for conventional SiO_2 in submicron MOS devices. These dielectrics are attractive for surface channel p^+-polysilicon gate p-MOSFETs, due to their improved barrier properties against boron penetration [1-5]. However, there is a trade-off between the barrier properties and hot-carrier reliability of NH_3-based oxynitride gate dielectrics [3]. Whereas high nitrogen concentration is required to prevent boron penetration, hydrogen incorporation resulting from heavy NH_3-nitridation required for this purpose deteriorates hot carrier reliability of these dielectrics. Consequently, N_2O-based gate dielectrics are attractive. Although significant work has been presented on the hot-carrier reliability aspects of N_2O-based gate dielectrics, relatively less attention has been given to the boron penetration problem [2]. Specifically, a comparison among various NH_3-based and N_2O-based gate dielectrics is missing. In this paper, we present a detailed comparison of barrier properties of various NH_3-based oxynitrides *vs.* N_2O-grown oxides. A new technique, which combines N_2O and NH_3 processing, is demonstrated to realize excellent boron stopping potential as well as excellent hot carrier reliability properties.

2. EXPERIMENTAL

Oxynitride gate dielectrics were fabricated by oxide growth in N_2O ambient, NH_3-nitridation of O_2-grown oxides and O_2 or N_2 anneal of NH_3-nitrided oxides. P-type substrates with (100) orientation were used. Tables I and II provide a summary of nomenclature used for these dielectrics and the respective processing conditions. After 4000 Å polysilicon deposition, BF_2 implants were performed at 50 keV to a dose of 5.5×10^{15} cm^{-2}. Post-implant drive-in was performed in N_2 at various temperatures for 30 min. High frequency and quasistatic C-V measurements were used to characterize the boron penetration.

3. RESULTS AND DISCUSSION

Fig. 1 shows normalized inversion capacitance ($C_{QS,inv}/C_{ox}$) of MOS capacitors with various gate dielectrics. The reduction of inversion capacitance below oxide capacitance (C_{ox}) is caused by depletion of polysilicon under this bias condition, due to insufficiently doped polysilicon gate. The smaller the $C_{QS,inv}/C_{ox}$ ratio, the larger is the polysilicon depletion effect. Thus, NH_3 and NH_3/N_2 samples show minimum polysilicon depletion among oxynitrides. Based on a model in [6], active dopant concentrations at the polysilicon/oxide interface were estimated for these devices and it is concluded that the concentrations are about 5X higher in NH_3 and NH_3/N_2 oxides as compared to control oxide. The reduction in the active dopant concentration at the polysilicon/oxide interface is possibly due to the diffusion of boron across the gate oxide during the drive-in anneal [5]. Accordingly, the suppressed polysilicon depletion in NH_3 and NH_3/N_2 oxides is attributed to nitrogen rich layer at the poly/SiO_2 interface, which suppresses the amount of boron from the p^+-doped polysilicon crossing the interface into the gate oxide.

Fig. 2 shows the quasi-static C-V curves for capacitors with different gate dielectrics. The C-V curve for control oxide is much distorted and shifted to higher V_g as compared to oxynitrides. The dramatic distortion of C-V curves in control oxides has been attributed to penetration of boron into the substrate and the formation of boron related defect centers [7]. Such distortion is not observed in the oxynitrides, indicating that the boron penetration is suppressed. Among oxynitrides, NH_3, NH_3/N_2 and NH_3/O_2 oxides show higher interface state density (D_{it}) than N_2O-oxides, as evidenced by the higher values of minimum C_{QS}. It has been reported that D_{it} is actually reduced due to the presence of fluorine

caused by BF_2 implantation [8]. Consequently, high values of D_{it} in NH_3, NH_3/N_2 and NH_3/O_2 oxides are attributed to the NH_3-nitridation step [9], rather than the effects of boron penetration.

Fig. 3 depicts flatband voltages (V_{fb}) of MOS capacitors with various gate dielectrics, for different post-implant anneal temperatures. It is observed that V_{fb} becomes more positive with increasing anneal temperature, except in the NH_3 and NH_3/N_2 samples. The V_{fb} shifts in positive direction are smaller in all oxynitride gate dielectrics than control oxide. Among oxynitrides, N_2O oxides show the largest V_{fb} shifts. NH_3, NH_3/O_2 and NH_3/N_2 oxides show significantly smaller V_{fb} shifts than control and N_2O oxides. Positive V_{fb} shifts in these capacitors can be attributed to a fully depleted layer of penetrated boron, located near the Si/SiO_2 interface [8]. The larger the amount of boron penetration, the larger are the positive V_{fb} shifts. Consequently, it can be concluded that all oxynitrides under investigation show suppressed boron penetration as compared to control oxides. Moreover, the ability to suppress boron penetration is much improved in NH_3, NH_3/O_2 and NH_3/N_2 oxides, as compared to N_2O oxides.

Reduced boron penetration in the substrate in NH_3, NH_3/N_2 and NH_3/O_2 samples can be attributed to the fact that the amount of boron crossing the poly-gate/SiO_2 interface, itself, is smaller in these samples. Strong nitrogen peaks at the Si/SiO_2 interface in these samples [9] further reduce boron penetration into the substrate, as suggested by Figs. 1 and 2. Nitrogen concentrations both at the Si/SiO_2 and the poly-gate/SiO_2 interfaces in N_2O oxides are, however, lower [2] as compared to NH_3, NH_3/N_2 and NH_3/O_2 [9]. These effects explain the larger V_{fb} shifts in N_2O oxides than the two NH_3-based oxynitrides. Nevertheless, a finite amount of nitrogen at the Si/SiO_2 interface results in a better suppression of boron penetration in N_2O oxides than the control thermal oxides. It is important to note that high nitrogen concentration near the poly-gate/SiO_2 interface, as seen in NH_3 and NH_3/N_2 samples, is crucial in suppressing polysilicon depletion effect as well as V_{fb} shifts due to boron penetration.

Although NH_3 and NH_3/N_2 show excellent ability to stop boron penetration, these dielectrics suffer from higher electron trapping [9,10]. On the other hand, although N_2O oxides and reoxidized NH_3-nitrided oxides show good hot carrier reliability [3,9,10], they are more susceptible to boron penetration, especially the polysilicon depletion effect. A new technique, namely NH_3-nitridation of N_2O-oxides (see Table II), is developed to achieve a highly reliable dielectric with excellent boron stopping potential.

To study the barrier properties of this new gate dielectric, V_{fb} values after a 30 min 900°C drive-in in N_2 ambient were compared with the corresponding V_{fb} values of control, N_2O and O_2/NH_3 oxides as shown in Fig. 4. It is evident that the boron stopping potential of N_2O/NH_3 oxides is significantly better than control and N_2O oxides and is comparable to that of O_2/NH_3 oxides. The oxide negative charge due to boron penetration was estimated from these V_{fb} values after correcting for oxide fixed charge, N_f [4]. These values are 9.8×10^{12}, 2.3×10^{12}, 5.6×10^{12} and 3.0×10^{12} cm^{-2} for control, $O2/NH_3$, N_2O and N_2O/NH_3 oxides, respectively. Thus, the amount of boron penetration in N_2O/NH_3 is only 30% of that in control and 50% of that in N_2O oxide. The improvement is attributed to the significant increase in the interfacial [N] due to NH_3-nitridation, as observed by SIMS.

Charge trapping properties of N_2O/NH_3 oxides were studied by monitoring the changes in gate voltage (ΔV_g) under a constant current density (-100 mA/cm^2) in MOS capacitors. As shown in Fig. 5, O_2/NH_3 oxides show a positive ΔV_g , indicating significant electron trapping by nitridation induced traps [9]. Nevertheless, even for 20 min NH_3-nitridation, N_2O/NH_3 oxides show only a small increase in electron trapping. ΔV_g in O_2/NH_3 oxides does not show a saturating trend, indicating a significant amount of high-field induced trap generation. On the contrary, despite a severe NH_3-nitridation, trap generation rate in N_2O/NH_3 oxides is negligible, resulting in superior charge trapping properties. Thus, it is possible to fabricate p-MOSFETs using these gate dielectrics, which show superior hot-carrier reliability, unlike p-MOSFETs with reoxidized NH_3-nitrided oxides which show worse reliability than those with conventional gate oxides [11]. These observations imply that the trade-off between sufficient [N] for better barrier properties *vs.* worse electron trapping can be greatly alleviated by this new technique of forming oxynitride gate dielectrics.

Fig. 6 shows Weibull plots for time-to-breakdown (t_{bd}) in n^+-polysilicon gated capacitors with different gate dielectrics. A large degradation in t_{bd} is observed in O_2/NH_3 oxides after 5 min NH_3-nitridation. The degradation in t_{bd} is usually attributed to large electron trapping in these oxides, apparent from Fig. 5. Contrary to such significant degradation in t_{bd} by NH_3-nitridation of pure oxides, 20 min NH_3-nitridation actually increased t_{bd} in N_2O-oxides to some extent. NH_3-nitridation for 5 min degraded charge-to-breakdown Q_{bd} (50% failure @ 100 mA/cm^2) in pure oxides from 50 C/cm^2 to 10.4 C/cm^2, while 20 min NH_3-nitridation improved Q_{bd} from 89 C/cm^2 to 118 C/cm^2 in N_2O-oxides.

Interface state generation (ΔD_{it}) due to constant current stress is plotted in Fig. 7. NH_3-nitridation increases ΔD_{it} in pure oxides. However, ΔD_{it} in N_2O/NH_3 oxides is comparable to the N_2O oxides. Large ΔD_{it} in O_2/NH_3 oxides is attributed to a distorted interfacial region due to the formation of mismatched Si-N bonds in the Si-O network. However, as seen from Fig. 7, nitrogen incorporation in N_2O oxides by NH_3-nitridation does not lead to such undesirable effect. This observation suggests that nitrogen incorporation at the interface by NH_3-nitridation of N_2O-oxides is somewhat different from that in pure oxides, and is currently under investigation.

4. CONCLUSION

In conclusion, a comparative study of boron stopping potential of various oxynitrides is presented based on both polysilicon depletion and V_{fb}-shift. It is concluded that NH_3 and NH_3/N_2 oxides show the highest resistance to boron penetration, although these dielectrics show worse hot-carrier reliability properties. To overcome this trade-off between barrier properties *vs.* hot-carrier reliability, a novel technique, namely NH_3-

nitridation of N_2O grown oxides, was suggested. It is demonstrated that this technique combines excellent hot carrier reliability of N_2O oxides and excellent boron stopping potential of NH_3-nitrided pure SiO_2 and is likely to play an important role in aggressively scaled dual gate CMOS technology.

5. REFERENCES

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Table I: Gate Dielectric (140 Å) Processing Details

Sample No.	Sample Name	Oxidation	NH_3-Nitridation	Post-Nitridation Anneal
1	Control	950°C, O_2 Ambient	-	-
2	N_2O	950°C, N_2O Ambient	-	-
3	NH_3	950°C, O_2 Ambient	950°C, 60 min	-
3	NH_3/N_2	950°C, O_2 Ambient	950°C, 60 min	950°C, 30 min, N_2 Ambient
4	NH_3/O_2	950°C, O_2 Ambient	950°C, 60 min	950°C, 30 min, O_2 Ambient

Table II: Gate Dielectric (80 Å) Processing Details

Sample No.	Sample Name	Oxidation	NH_3-Nitridation
5	Control	950°C, O_2 Ambient	-
6	N_2O	950°C, N_2O Ambient	-
7	NH_3	950°C, O_2 Ambient	900°C, 5 min
8	N_2O/NH_3-1	950°C, N_2O Ambient	900°C, 10 min
9	N_2O/NH_3-2	950°C, N_2O Ambient	900°C, 20 min

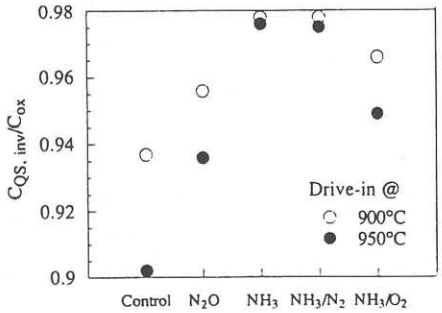

Fig. 1 Polysilicon depletion effect, as monitored by normalized inversion capacitance ($C_{QS,inv}/C_{ox}$) in various gate dielectrics.

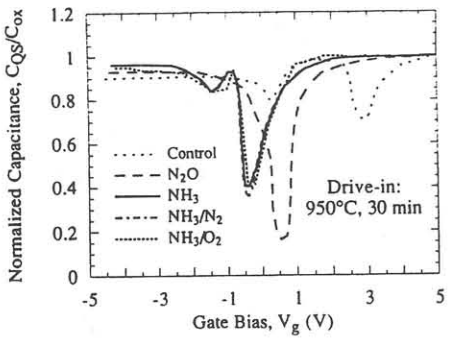

Fig. 2 Normalized quasi-static C-V curves for MOS capacitors with control and various oxynitride gate dielectrics.

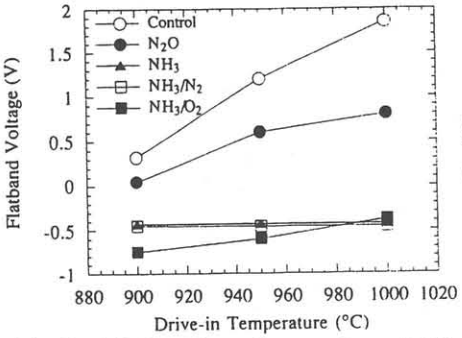

Fig. 3 Flatband voltage for MOS capacitors with different gate dielectrics as a function of post-implant drive-in temperatures.

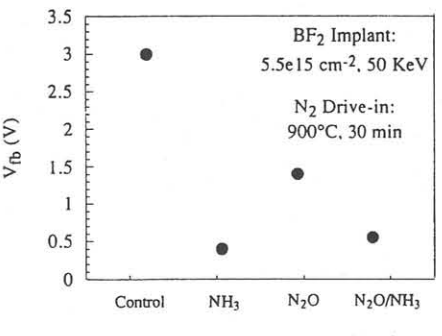

Fig. 4 Flatband voltage in BF_2-implanted p^+-polysilicon gate MOS capacitors with different gate dielectrics.

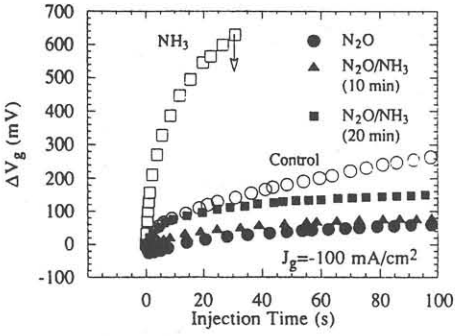

Fig. 5 Changes in gate voltage required to maintain a constant current density of -100 mA/cm^2 in MOS capacitors (area: 5x10^{-4} cm^2) with different gate dielectrics.

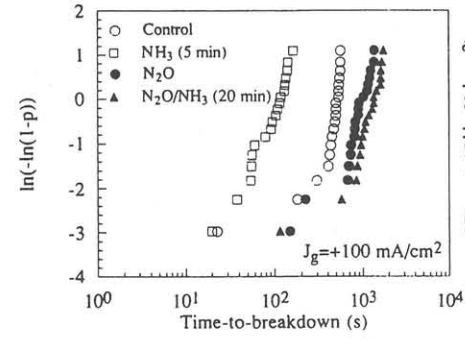

Fig. 6 Weibull plots of time-to-breakdown in MOS capacitors (area: 5x10^{-5} cm^2) with different gate dielectrics at a current density of 100 mA/cm^2.

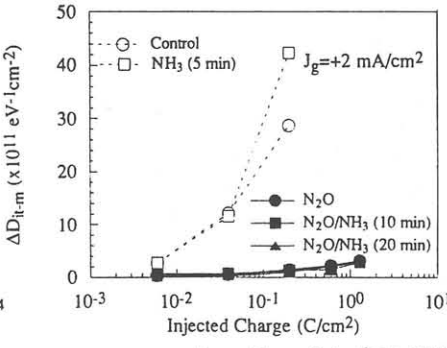

Fig. 7 Increase in midgap interface state density (ΔD_{it-m}) in MOS capacitors (area: 5x10^{-4} cm^2) with different gate dielectrics, caused by F-N injection at 2 mA/cm^2 with positive gate bias.