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A Novel LOCOS-Type Isolation Technology Free of the Field Oxide Thinning Effect

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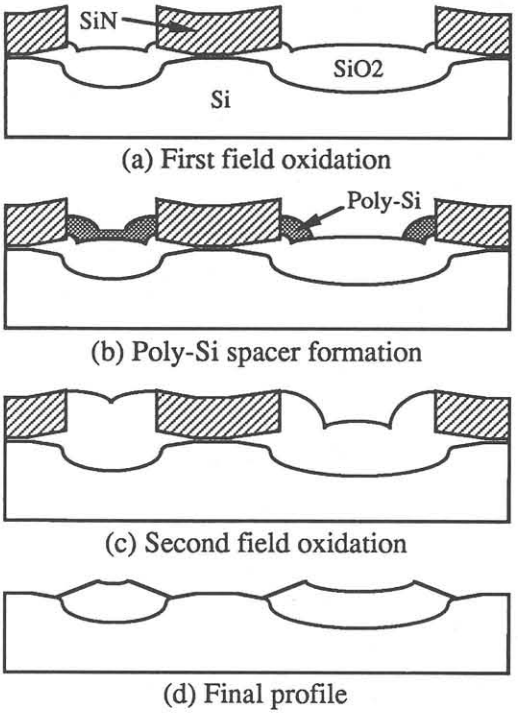
A novel LOCOS-type isolation technology named POlysilicon Spacer LOCOS (POS-LOCOS) has been developed. After the first field oxidation, poly-Si is deposited and etched unisotropically. Then the second oxidation is performed by oxidizing the poly-Si spacers. POS-LOCOS eliminates the field oxide thinning effect. Devices with POS-LOCOS show lower peripheral junction leakage current and higher field transistor threshold voltage compared to the conventional LOCOS isolation.

1. INTRODUCTION

In LOCOS-type isolation technologies, the field oxide thickness decreases as the isolation size is reduced. This field oxide thinning effect [1] is one of the factors that limit the application of the LOCOS-type isolation to the deep-submicron devices. In this study, a novel LOCOS-type isolation, POlysilicon Spacer LOCOS (POS-LOCOS), that eliminates the field oxide thinning effect has been developed.

2. EXPERIMENTAL

The process sequence of POS-LOCOS is shown in Fig. 1. After windows for the field region are opened and the silicon substrate is etched for the recessed field oxide, the first field oxidation is carried out (Fig. 1 (a)). Then the poly-Si film is deposited and etched unisotropically (Fig. 1 (b)). At the narrow field region, substantial amount of poly-Si remains after etching, while only spacers are formed at the ends of the field region for the wide region, as schematically illustrated in Fig. 1 (b). The second field oxidation is performed to oxidize the poly-Si layer (Fig. 1 (c)).



(a) First field oxidation

(b) Poly-Si spacer formation

(c) Second field oxidation

(d) Final profile

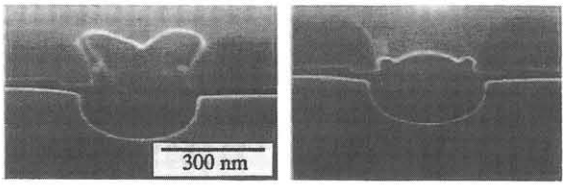
Figure 1. Process steps for POS-LOCOS.

3. RESULTS AND DISCUSSIONS

Figures 2 (a) and (b) show cross-sectional SEM micrographs of POS-LOCOS and conventional LOCOS, respectively, after the conventional LOCOS, respectively, after the second field oxidation. Here, SiN spacers were formed to reduce the isolation size and poly-Si was deposited to a thickness of 300 nm. The field oxide thinning effect can be compensated by the second oxidation because thicker oxide is obtained as the field oxide width becomes narrower.

SEM micrographs in Fig. 3 compare the final isolation profiles of POS-LOCOS and conventional recessed LOCOS for the drawn isolation sizes of 0.35 μm and 0.6 μm. One notes that in the narrow field region, substantially thicker field oxide was obtained with POS-LOCOS. Figure 3 also shows that with POS-LOCOS, lateral encroachment is reduced compared to LOCOS. This is because in POS-LOCOS, bird's beak is grown during the first oxidation only. The final field oxide thickness as a function of the isolation size shown in Fig. 4 confirms that POS-LOCOS eliminates the field oxide thinning effect. This leads to an improvement of the threshold voltages of field transistors, as shown in Fig. 5.

Figure 6 shows that the leakage current level of the N^+/P junction with POS-LOCOS is lower than that of conventional LOCOS. The probable cause is lower stress level associated with field oxidation. It is expected that only the field oxidation step which oxidizes the silicon substrate will generate significant stress. The NMOS transistor with POS-LOCOS shows a normal behavior, with low leakage current, as shown in Fig. 7.



(a) POS-LOCOS (b) Recessed LOCOS

Figure 2. Cross-sectional SEM after the second oxidation. Depth of the recess etching was 60 nm and the first and the second oxidation thicknesses were both 200 nm.

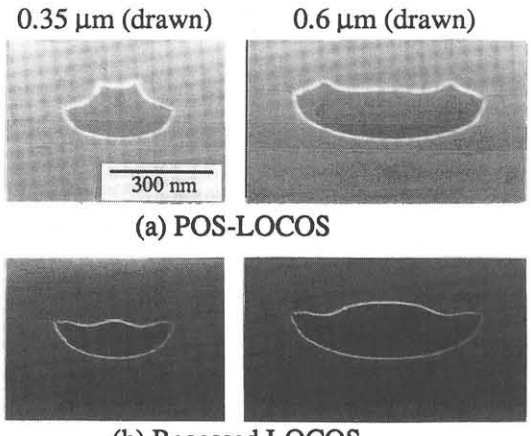


Figure 3. SEM of the final isolation profile.

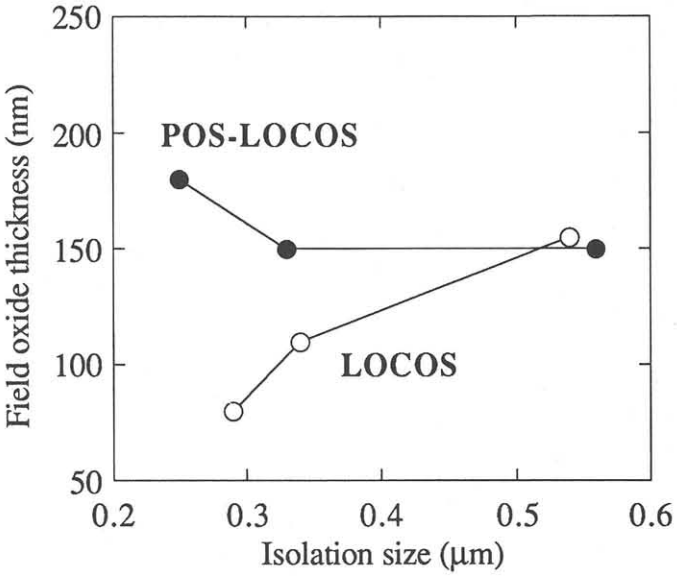


Figure 4. Field oxide thicknesses with respect to the isolation size. The first and the second oxidation thicknesses were both 200 nm at wide isolation regions for POS-LOCOS, and the same oxidation steps were carried out for conventional recessed LOCOS.

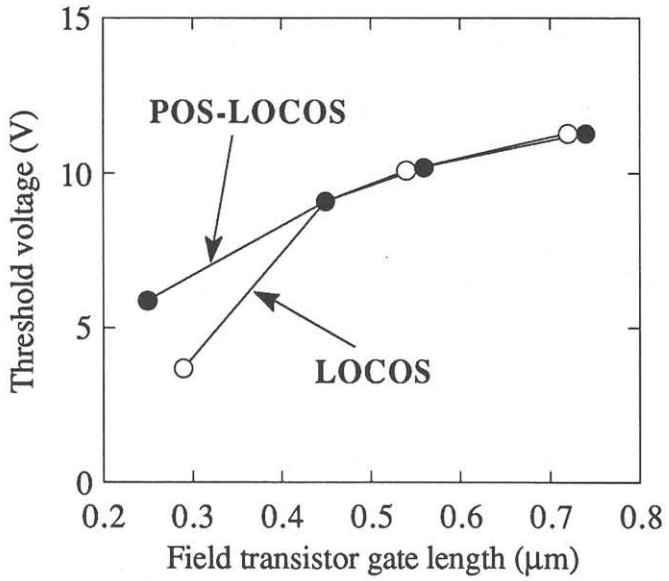


Figure 5. Threshold voltages (V_t) of field transistors according to the isolation size. W is 100 μm, V_d and V_{sub} are 3.3 V, 0 V, respectively. V_t was defined as the gate voltage when I_d = 1 μA.

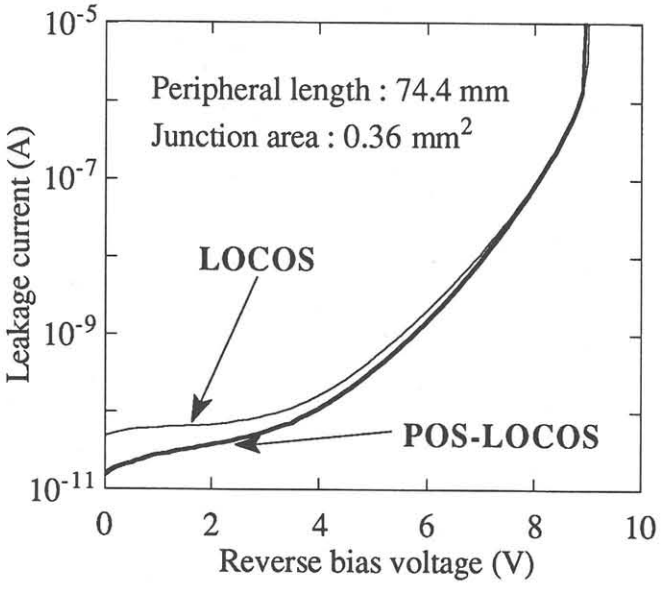


Figure 6. Junction leakage currents of the N^+/P junctions with LOCOS and POS-LOCOS.

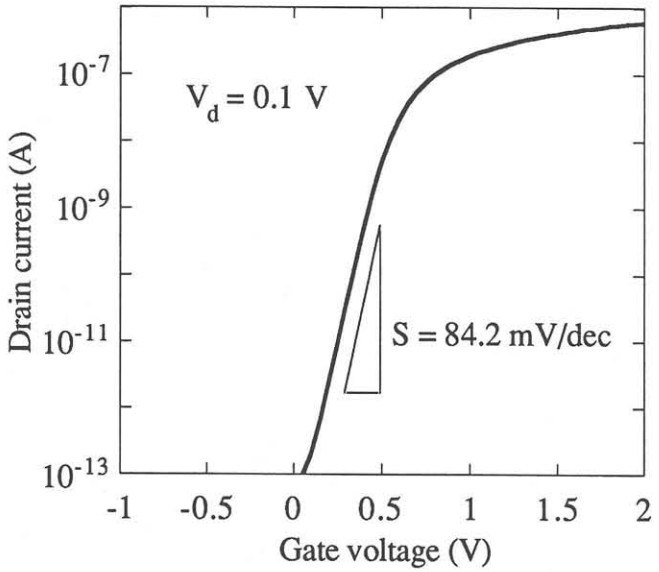


Figure 7. I_d-V_g characteristic of an NMOSFET with L = 10 μm and W = 0.3 μm at V_d = 0.1 V, and V_{sub} = 0 V. Gate oxide thickness is 8 nm.

4. CONCLUSION

In summary, with POS-LOCOS, it is possible to overcome the field oxide thinning effect with a simple fabrication process. POS-LOCOS also reduces the lateral encroachment and the junction leakage current. It is expected that POS-LOCOS will help extend the lifetime of the LOCOS-type isolation to the next generation of the IC technology.

REFERENCE

1. T. Mizuno et al., "Oxidation Rate Reduction in the Submicron LOCOS Process" *IEEE Trans. Elect. Dev., Nov. 1987, p.2255.*