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Thermal Analysis of Laser-Emission Surface-Normal Optical Devices with a Vertical Cavity

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Laser-emission surface-normal optical devices with a vertical cavity are expected to be key devices for optical interconnections. Thermal characteristics improvement is necessary for large-scale two-dimensional array integration which increases the number of optical interconnections. To optimize the device structures for thermal characteristics, it is needed to know the temperature rise of DBRs and active layer. Here, we report first temperature rise evaluation in both regions, and it is found that the temperature rise is small for a compact double mesa structure which allows a single lateral mode oscillation.

1. Introduction

For photonic switching and optical information processing, two-dimensional (2-D) optical interconnect systems[1], which can allow a lot of channels, have been extensively studied. Under these circumstances, laser-emission surface-normal optical devices with a vertical cavity are expected to be key devices for optical interconnections. Highly efficient CW operation and thermal characteristics improvement are necessary for large-scale 2-D array integration which increases the number of channels. Highly efficient CW operation enables devices to operate at low power consumption. Thermal characteristics improvement is required to reduce the thermal influence from surrounding devices. In order to optimize the device structures for good thermal characteristics, we must know the temperature rises in both DBRs and active layer. They may be different, but have not been measured yet. Here, we report results on the first evaluation of the temperature rises in both regions for various device structures. It is found that the temperature rise is small for a double mesa structure, even in a small size which allows a single lateral mode oscillation.

2. Device Structure

Two types of device structures shown in Fig. 1 are adopted for the measurements and the simulation. All of these are Vertical to Surface Transmission Electro-Photonic devices with vertical cavities (VC-VSTEPs)[2-4]. VSTEPs are based on a concept of a fusion of electronics and photonics in a device level[5]. These VSTEPs have several functions such as light emission, light detection, memory, and logical

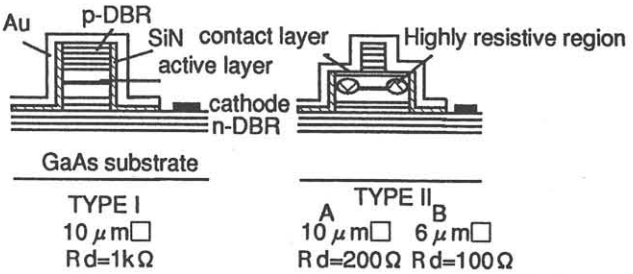

Fig. 1 Device structure used in the simulations and measurements. Rd denotes a differential electrical resistance during on state of the VSTEPs.

operation. VC-VSTEPs work as surface emitting laser in the on-state. Recently, to improve detector characteristics, a variation of the original VC-VSTEP consisting of a double-cavity-detector and a single-cavity-laser sections has been also proposed[6].

In Fig. 1, Type I is a single mesa structure, in which the current is injected through a top-DBR. Type II is a double mesa structure[3,4], in which the current is injected through a contact layer without flowing through a top-DBR. In addition, in Type II devices, the proton implanted region is formed for effcient confinement of carriers in the active layer, which leads to highly efficient operation. The number of DBR pairs is the same in both Type I and Type II devices, which is 15 pairs for a top-DBR, and 18.5 pairs for a bottom-DBR. The top-mesa size of each device is shown in Fig. 1. Also, the differential electrical resistance of each device in the on-state is shown in Fig. 1. The Type II-B device has a low

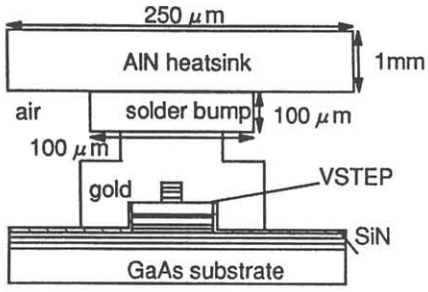

Fig. 2. Schematic view of the model using the simulations.

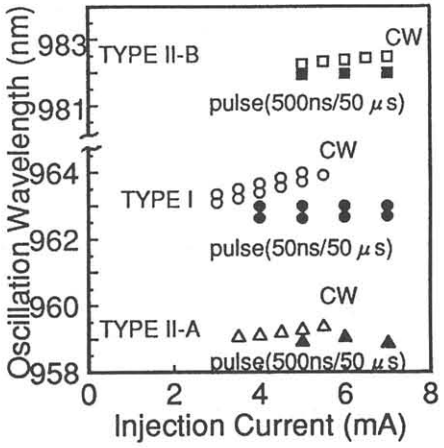

Fig. 3. Injection current vs. oscillation wavelength plot for each device (TYPE I-II)

Table 1. Thermal conductivity of each material used in the simulation.

material	thermal conductivity κ (W/K · cm)
$Al_xGa_{1-x}As$	$0.44/(1+12.7x-13.22x^2)$
$In_{0.2}Ga_{0.8}As$	0.412
gold	3.18
Sn/Pb solder bump	0.51
AlN heatsink	2.41
SiN	0.1
air	2.61×10^{-4}

electrical resistance due to a reduction in contact resistance by zinc diffusion (570°C, 7 minutes).

3. Simulation

The temperature distribution is simulated by the thermal conductivity equation, using the finite element method. The model of this simulation is shown in Fig. 2, which is based on the measured devices with heatsinking. The thickness of gold is 9μm, and that of SiN is 0.2μm. The pitch between VSTEPs is 250μm for Type I and Type II-A devices, and 125μm for Type II-B device. Each device is fabricated on a GaAs substrate, and flip-chip bonded onto an AlN subcarrier (heat sink) through a Sn/Pb solder bump. The temperature for a top surface of the heat sink is fixed to 20°C. The size of each part is in accordance with the measured devices. The thermal conductivity κ of each material is shown in Table 1[7]. The spacer layers consist of $Al_{0.25}Ga_{0.75}As$ and $Al_{0.4}Ga_{0.6}As$. The active layer is $In_{0.2}Ga_{0.8}As$. The DBRs consist of AlAs/GaAs quarter-wave stacks with linearly graded transition layers. Considering the injection current path, the heat sources are the top-DBR and the active layer for Type I device, and, on the other hand,

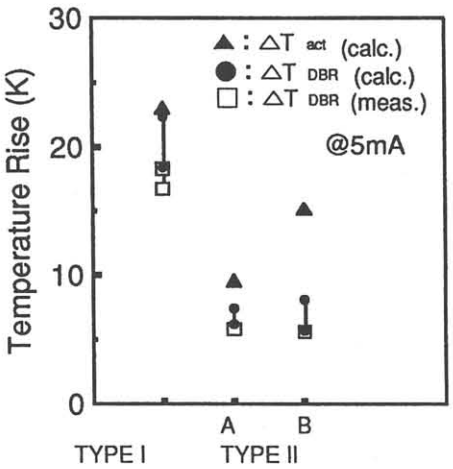

Fig. 4. Temperature rise of each device. ΔT_{act} denotes the temperature rise of active layer; and ΔT_{DBR} denotes that of DBRs.

the contact layer and the active layer for Type II devices. The heat power given in the above heat sources is $V_H \times I$ (V_H: holding voltage, I: injection current) for the active layer, and $P - (V_H \times I) - P_{out}$ (P: input power, P_{out}: light-output power) for the top-DBR or the contact layer. In this simulation, injection current I is assumed to be 5mA. The holding voltage

V_H is about 2V from I-V characteristics of each device.

The simulated results for each device structure are shown in Fig. 4. In Fig. 4, the temperature rise of top-DBR ΔT_{DBR} and that of active layer ΔT_{act} is shown. There is little difference between the temperature distribution of the top-DBR and that of the bottom-DBR, so that, here, the temperature rise of the top-DBR is adopted as those of DBRs. Since the temperature inside DBRs changes along the direction of the DBR, the value of ΔT_{DBR} has some widths.

4. Measurement

Each device is flip-chip bonded onto an AlN heat sink, and the temperature of the heat sink was controlled to be 20°C by Peltier element. The DBR temperature rise for each device is estimated from the oscillation wavelength differences between CW and pulsed operations. Here, it is assumed that the wavelength shifts at a rate of 0.6 Å/K[8] due to the DBR temperature rise.

Figure 3 shows the dependence of oscillation wavelength λ on injection currents I for CW and pulsed operations. In pulsed operations, the pulse width / duty cycle are 50ns/50μs for Type I device and 500ns/50μs for Type II devices, respectively as shown in Fig. 3. From these results shown in Fig. 3, the DBR temperature rise ΔT_{DBR} for I=5mA is calculated as shown in Fig. 4. Although the pulse width for Type I (50ns) is less than that of Type II (500ns), the DBR temperature rise ΔT_{DBR} of the Type I device was higher than that of the Type II devices.

In Fig. 3, two oscillation wavelengths are, in some cases, plotted for one injection current, which means that two-mode oscillation were obserbed.

5. Results and Discussion

The measured results are compared with the simulated results obtained using a finite element method. The simulated results for DBR temperature rise for each device are consistent with the measured results as shown in Fig. 4. These results indicate that the temperature rise in the active layer of each device is estimated from the simulation.

The temperature rise of the active layer of the Type II device is less than that of the Type I device by at least a factor of two. From this result, it is found that the double mesa structure [2),3)] is better for a reduction of device temperature and high integration.

Moreover, as for device size, the temperature rise of the active layer in the Type II-B device with a lower electrical resistance is about only 1.5 times higher than that in the Type II-A device. Considering the scaling rule, that temperature rise should be about 3 times higher. This means that thermal resistance saturation together with the effect of electrical resistance reduction results in reducing the temperature rise of the device.

In order to prevent the influences of the thermal crosstalk between devices, we should operate these devices at less than a few mA. Therefore, a threshold current should be less than about 1mA, and a light output power should be more than about 100 μW at a few mA. It will be important to design devices which satisfy the above requirements. This will be described in detail elsewhere[9].

6. Conclusion

In conclusion, the temperature of the active layer is estimated from both measured and calculated results for the first time. Furthermore, a device is fabricated with low electrical resistance by zinc diffusion and it is confirmed that temperature decrease in the device is due to a saturation in thermal resistance and a reduction in electrical resistance.

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References

1) K. Kasahara, IEEE J. Quantum Electron. **29**, (1993) 757.
2) T. Numai, M. Sugimoto, I. Ogura, H. Kosaka, and K. Kasahara, Appl. Phys. Lett. **58**, (1991) 1250
3) T. Numai, K. Kurihara, I. Ogura, H. Kosaka, M. Sugimoto, and K. Kasahara, IEEE Photon. Technol. Lett. **5**, (1993) 136
4) K. Kurihara, T. Numai, I. Ogura, H. Kosaka, M. Sugimoto, and K. Kasahara, Jpn. J. Appl. Phys. **32**, (1993) 604
5) K. Kasahara, Y. Tashiro, N. Hamao, M. Sugimoto, and T. Yanase, Appl. Phys. Lett. **52**, (1988) 679
6) H. Kosaka, I. Ogura, M. Sugimoto, H. Saito, T. Numai, and K. Kasahara, Jpn. J. Appl. Phys. **32**, (1993) 600
7) S. Adachi, J. Appl. Phys. **54**, (1983) 1844
8) B. Tell, K.F. Brown-Goebeler, and R.E. Leibenguth, IEEE Photon. Technol. Lett. **4**, (1992) 521
9) M. Kajita, T. Numai, K. Kurihara, M. Sugimoto, I. Ogura, H. Kosaka, and K. Kasahara, to be submitted to Jpn. J. Appl. Phys.