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A New GaAs FET with δn-δp DIpole Barrier(DIB)

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A new GaAs FET with DIpole-Barrier(DIBFET) employing a delta-n(δ_n) layer and a delta-p(δ_p) layer is proposed and fabricated. Electrons are confined in the upper undoped-GaAs layer rather than the δ_n layer by the influence of the transverse electric field resulting from the dipole-barrier formation. This leads to the high electron concentration of $1.5\times10^{18}cm^{-3}$ with the electron mobility of $3600cm^2/V\cdot sec$ in the undoped GaAs at room temperature. The fabricated GaAs DIBFET with 0.8μm gate length shows the maximum value of extrinsic transconductance of 366mS/mm. The drain current density at the gate voltage of 0V is about 550mA/mm. The high values of the transconductance and current density are viewed as a result of the enhanced transport property in the channel. The current gain cutoff frequency f_T of 16.7GHz and the maximum oscillation frequency f_{max} of 67GHz are obtained.

I. Introduction

GaAs FETs employing delta(δ)-doped layers have been reported, taking advantage of high current density, improved linearity in transfer characteristics, high transconductance, and high breakdown voltage[1-3]. However, the electron mobility value in the δ-doped layer is rather low due to the localized high doping density and the consequent high ionized impurity scattering rate[4]. In this paper, a new GaAs FET with DIpole Barrier (DIBFET) adopting a delta-n(δ_n) layer and a delta-p(δ_p) layer is proposed and fabricated, where electrons are confined in the upper undoped-GaAs layer rather than around the δ_n layer by the influence of the transverse electric field coming from the dipole-barrier formation. This results in the high electron drift mobility in the channel layer. The high current density and transconductance due to the enhanced transport property is demonstrated. Furthermore, the very low substrate current is expected because of the high potential barrier between the channel and the buffer layer.

II. Epitaxial Growth and Device Fabrications

The schematic illustration of the proposed structure is shown in Fig.1(a). In Fig.1(b), the schematic of electron concentration and electrostatic potential profile with respect to Fermi-level is displayed, which is obtained from one-dimensional analysis.

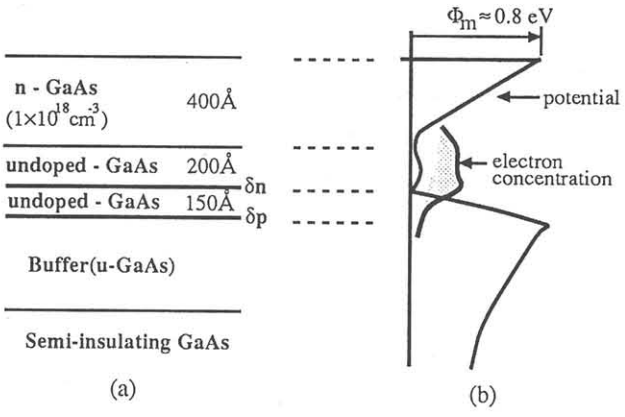

Fig 1. (a) The layer structure of GaAs DIpole-Barrier (DIB)FET and (b) the schematic of electron concentration and potential profile with respect to Fermi-level from one-dimensional analysis. ($\delta_n=5\times10^{12}cm^{-2}$, $\delta_p=3\times10^{12}cm^{-2}$)

All the layers in the structure are grown by Atmospheric-Pressure Metal Organic Chemical Vapor Deposition(AP-MOCVD). The growth rate is about 400Å/min, the growth temperature is 650°C and V/III ratio is 15. The 0.5μm thick undoped GaAs layer is firstly grown as a buffer layer. The δ_p layer with the estimated doping density of $3\times10^{18}cm^{-3}$ and the thickness of 80Å is subsequently grown. Carbon is used as the p-type dopant in the δ_p layer. The dopant(carbon) has the smaller diffusion coefficient in GaAs than the other dopants such as Zn and Be[5]. A δ_n layer is grown by using the atomic layer doping technique[1], following the 150Å thick undoped GaAs spacer layer. The source of Si as the n-type dopant in the δ_n-layer is 60ppm SiH_4 diluted by H_2. The gas flow-rate of SiH_4 is 25sccm and to have a doping duration is 60sec. The δ_n layer is estimated the peak electron density of $1\times10^{19}cm^{-3}$ and a Full Width Half Maximum(FWHM) of 50Å. The FWHM is obtained from a C-V measurement. The thicknesses of the undoped channel layer over the δ_n layer and the n-capping layer with the doping density of $1\times10^{18}cm^{-3}$ are 200Å and 400Å, respectively. The n-capping layer is almost depleted by the built-in potential of the Schottky gate metal. The electron density and electron drift mobility profile obtained from the C-V and FATFET measurements are shown in Fig.2, where the peak electron density of 1.5×10^{18} cm^{-3} and the peak electron drift mobility of 3600 $cm^2/V\cdot sec$ in the undoped channel layer are exhibited. It is found in the figure that electrons are confined in the upper undoped-GaAs layer rather than around the δ_n layer by the influence of the transverse electric field resulting from the dipole-barrier formation.

AuGe/Ni/Au is evaporated and the subsequent rapid thermal alloying at 430°C is carried out for the ohmic contacts. The specific contact resistance obtained from TLM measurement is smaller than $1\times10^{-6}\Omega\cdot cm^2$. Devices are isolated by mesa etching with NH_4OH :H_2O_2:H_2O solution. A Schottky gate is formed by the thermal evaporation of Aluminum and the lift-off process.

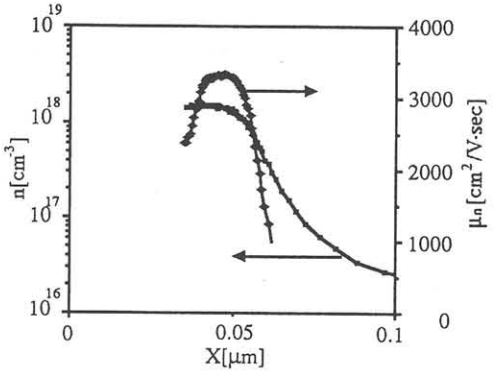

Fig 2. Electron concentration and electron drift mobility profile obtained from C-V and FATFET measurements. The abscissa is the distance from gate.

III. Device Characteristics

The drain output characteristics and transfer characteristics of DIBFET with the gate length of 0.8μm and the gate width of 30μm are shown in Fig.3(a) and (b), respectively. The maximum extrinsic transconductance of 366mS/mm and the current density of 550mA/mm at zero gate voltage are obtained. The current density is

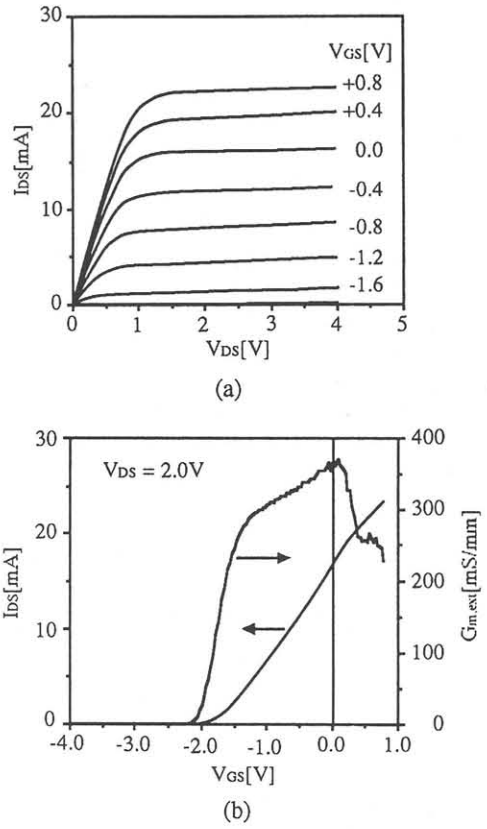

Fig.3 (a) Drain characteristics and(b) transfer chracteristics of the fabricated GaAs DIBFET
(L_G = 0.8 μm , W_G = 30 μm)

larger than 800mA/mm at the gate voltage of +0.6V. The output resistance at zero gate bias is 171Ω·mm. The S-parameters are measured on a device with the gate length(L_G) of 0.8μm and the gate width(W_G) of 100μm using a cascade microprobe and a HP-8510 network analyzer. Fig.4 shows the current gain cutoff frequency f_T of 16.7GHz and the maximum oscillation cutoff frequency f_{max} of 67GHz at V_{GS}=0V and V_{DS}=2V. The high value of f_{max} reflects the high output resistance in the device. Fig.5 shows the small-signal equivalent circuit of the DIBFET(L_G=0.8μm; W_G=100μm) at the same bias.

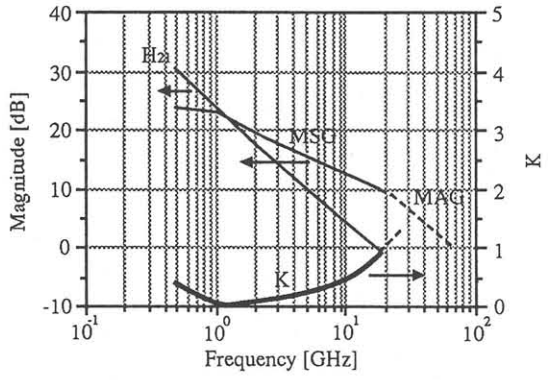

Fig 4. Measured frequency charateristics of GaAs DIBFET with L_G = 0.8 μm and W_G = 100μm
(F_t = 16.7 GHz , F_{max} = 67GHz)

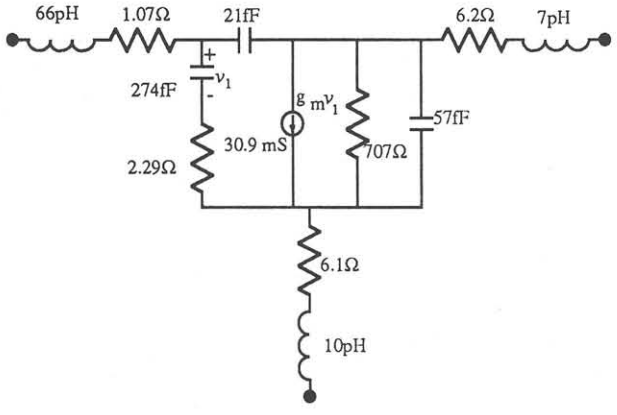

Fig.5 Small-signal equivalent circuit of DIBFET

IV. Conclusion

We have proposed and fabricated a new GaAs FET with a dipole-barrier (DIBFET). The GaAs DIBFET shows the improved DC characteristics due to the confinement of electrons in the undoped channel layer with the high electron drift mobility. It comes from the effect of the transverse electric field due to the dipole-barrier formation . The high value of f_{max} reflects the high output resistance, which is also caused by the prevention of substrate conduction due to the high potential barrier between the channel layer and the buffer layer.

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