Extended Abstracts of the 1993 International Conference on Solid State Devices and Materials, Makuhari, 1993, pp. 742-744

Process Induced Defects in InP Produced by Chemical Vapor Deposition of Surface Passivation Dielectrics

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Process induced near-surface defects of InP produced during three different CVD processes were systematically characterized by *C-V* and DLTS techniques. Deposition of PECVD phosphosilicate glass (PSG) and SiO_2 films introduced the same bulk level, lying at 0.35eV below Ec, near surface region of InP. Such a level was absent in the samples by Photo-CVD process. In addition, Photo-CVD process gives lower density of interface states than the PECVD process. The origin of the bulk trap and behavior of interface states were discussed.

1. Introduction

Surface passivation is a crucial processing step for fabrication of advanced InP electronic and optoelectronic devices. Utilization of a chemical vapor deposition (CVD) technique is a standard approach. However virtually nothing is known on near surface defects produced during CVD processes.

The purpose of the present paper is to systematically characterize process induced defects in InP surface introduced during different CVD processes for surface passivation. Capacitance-voltage (*C-V*) and DLTS techniques were applied to passivated MIS samples and near-surface defects were detected by changing the bias condition. It is unambiguosly shown that CVD processes introduce both of discrete traps and interface states, and that photo CVD (Photo-CVD) process produces much less damage than plasma enhanced CVD (PECVD) process.

2. Experimental

The CVD processes investigated here are summarized in Table 1. In order to investigate the effect of the presence of phosphorous on the surface damage of InP during deposition process, phosphosilicate glass (PSG) films were prepared by high-frequency (27MHz) PECVD at 300 ℃ from a mixture of SiH_4, N_2O and P_4. Phosphorous content in PSG films was varied from 2 to 40% using XPS monitoring. SiO_2 films were deposited either by low-frequency (50Hz) PECVD[1)] at 40-200 ℃ or by mercury sensitized Photo-CVD at 130 ℃ using a mixture of SiH_4 and N_2O. The typical deposition rate and thickness of films were 5nm/min and 100nm, respectively.

Table 1. Summary of CVD process.

	Deposition method	Deposition temperature	Remarks
PSG/InP	PECVD	300℃	P: 2wt%
PSG/InP	PECVD	300℃	P:14wt%
PSG/InP	PECVD	300℃	P:40wt%
SiO_2/InP	PECVD	40℃	50Hz
SiO_2/InP	PECVD	200℃	50Hz
SiO_2/InP	Photo-CVD	130℃	Mercury-sensitized

Wafers used in the present work were undoped n-type liquid encapsulated Czochralski (LEC) InP with a carrier concentration of $5x10^{15}cm^{-3}$. InP surface was treated in HF solution prior to deposition process.

3. Results and Discussion

Typical DLTS spectra obtained for the PSG/InP MIS samples are shown in Fig.1. By systematically changing bias pulse conditions in DLTS study, clear distinction between bulk traps and interface states was made possible as shown in Fig.1. The surface potential change between injection and emission pulses was carefully controlled so that it becomes constant at each quiescent bias. In Fig.1, the DLTS peak position at around 200K was independent of the bias and remained at the same temperature, corresponding to a constant

emission time constant from a discrete bulk level. On the other hand, the other peak moved continuously with bias,[2] indicating that it is due to interface states which sensitively reflect bias-induced changes in surface potential and emission time constants of responding states. Note that the DLTS peak at the bias of -0.7/-1.0V contains both signals from the bulk level and interface states.

DLTS spectra after three CVD processes are compared in Fig.2. PECVD deposition of PSG and SiO_2 films produced the same discrete level with the concentrations in the range of 10^{13}-$10^{14}cm^{-3}$. A DLTS study using a Schottky diode indicated that no such level was present in InP before PECVD process. It was also absent in the samples by Photo-CVD process. Furthermore, the bulk level was present only in the vicinity of the surface, within about 200nm, which was estimated from the depletion capacitance of InP at the bias where the DLTS peak of the level disappeared. Thus, these observations clearly indicated that this level is process-induced defect level.

Figure 3 gives the Arrhenius plots of the bulk level and interface states. The bulk trap introduced by PECVD process is located at 0.35eV below conduction band edge, Ec, with a capture cross section in the range of $10^{-16}cm^2$.

The concentration of the observed bulk trap was found to decrease with the increase of the phosphourous content in PSG films as shown in Fig.4, in spite of the fact that the interface state density (Nss) distributions were almost the same in three PSG/InP samples with different P contents. Ninomiya *et al.*[3] recently reported that the process-induced defect level in the InP surface region exposed to H_2 and Ar plasma was much reduced by PH_3 plasma treatment. The "signature plots" of the level is very close to those of the reported defect level, as shown in Fig.3. They suggested that the formation of thin phosphorus

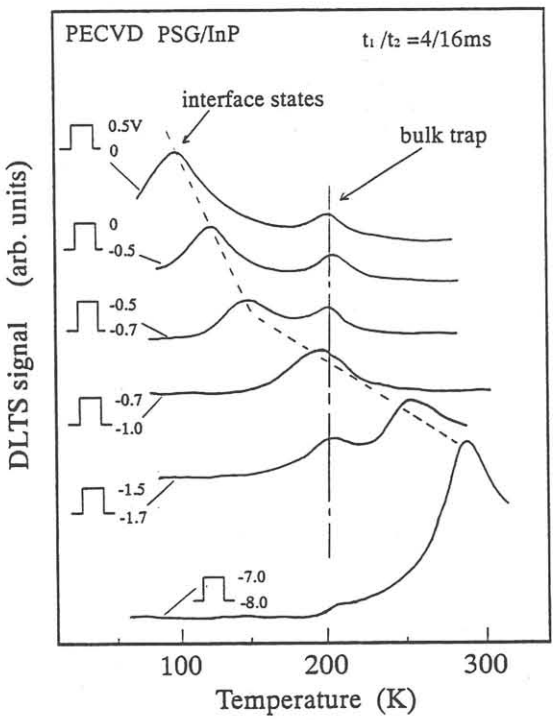

Fig.1. DLTS spectra under small bias swings for PSG/InP systems.

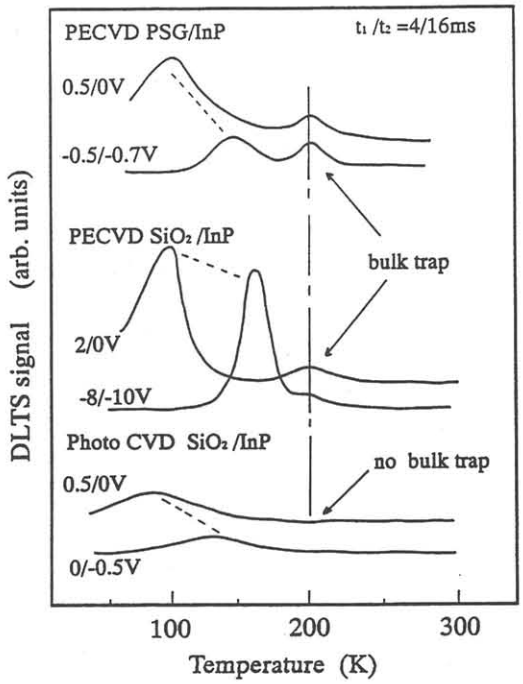

Fig.2. DLTS spectra for three different InP MIS systems.

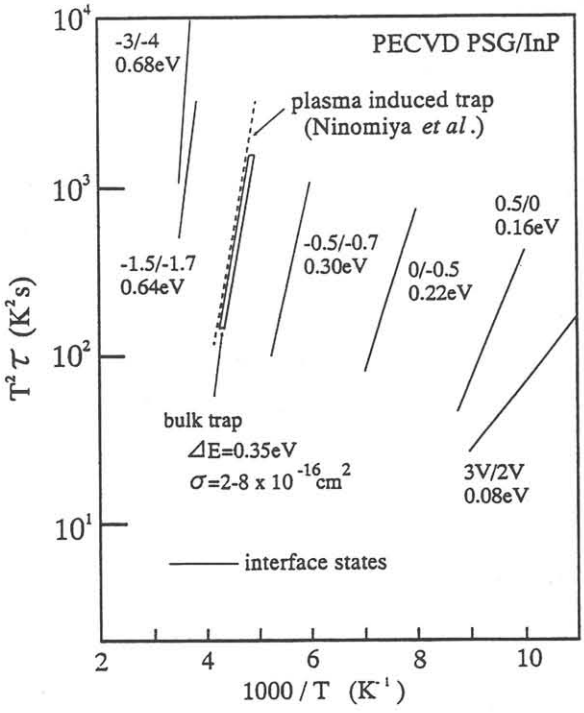

Fig.3. Arrhenius plots of the bulk trap and interface states for PSG/InP system.

layer at InP surface during PH_3 plasma treatment was effective in suppressing surface damage related to phosphorous vacancy. The results indicated in Fig.4 support this suggestion. Thus, it is likely that the observed bulk level is related to phosphorous vacancies or their complexes created during PECVD process.

DLTS results in Fig.2 clearly show that the interface state density for InP MIS systems is very much processing-dependent. Nss distribution determined by *C-V* and DLTS techniques are compared in Fig.5 for three CVD processes.

Both *C-V* and DLTS results gave similar U-shaped continuous distributions with nearly the same energy position of minimum density, being consistent with the disorder-induced gap-state (DIGS)[4] model. It is also shown in Fig.3 that activation energies change with bias conditions in a consistent way with a continuous distribution of Nss. As for the magnitude of Nss, on the other hand, the DLTS result showed smaller values than the *C-V* result especially near Ec.

This discrepancy in the magnitude of Nss can be explained in terms of the space and energy distributed nature of interface states in accordance with the DIGS model.[4] When states are distributed both in energy and space, *C-V* sampling by surface potential becomes different from DLTS sampling by the emission time constant. The farther the states are situated from the interface, the smaller becomes their emission rate even they have the same energy position. This difference becomes larger at low temperatures where the emission rate of the states near Ec meets the setting rate window in DLTS method, about $100s^{-1}$ in the present work, than at room temperature where the *C-V* measurements were done. Therefore, DLTS measurements tend to underestimate Nss near Ec rather than Nss near midgap of which DLTS signal goes through maximum at around room temperature. The fact that such a discrepancy has been barely seen in SiO_2/Si systems prepared by thermal oxidation of Si reflects the fact that the spatial distribution of Nss is much reduced compared with the deposited MIS systems.

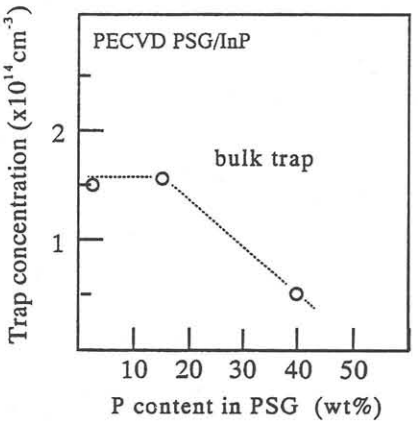

Fig.4. The trap concentration of bulk level versus P content in PSG for PSG/InP system.

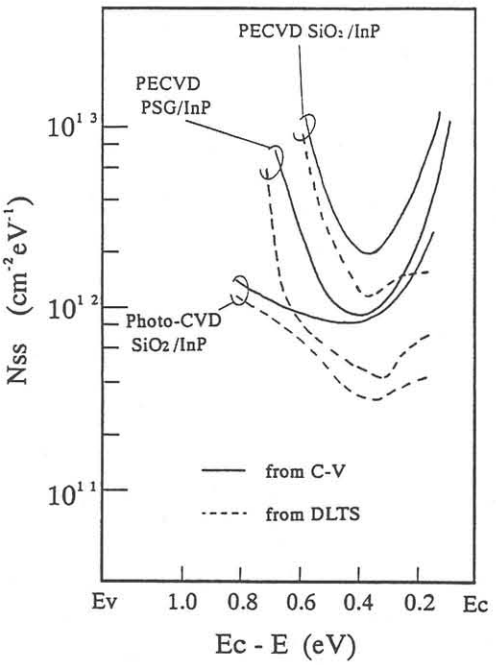

Fig.5. Nss distribution for the PSG/InP and SiO_2 /InP systems.

4. Conclusions

Process-induced near-surface defects of InP introduced during CVD processes were systematically characterized by DLTS and *C-V* techniques. Deposition of PECVD PSG and SiO_2 films produced the same bulk trap, lying at 0.35eV below Ec, whereas no such level was present in the samples by Photo-CVD process. This level is probably related to phosphorous vacancies or their complexes due to plasma damage. Both DLTS and *C-V* results showed that the magnitude of the interface states density is also very much processing-dependent. Photo-CVD process gave lower densities of states than the PECVD process. The discrepancy between Nss distribution from DLTS and *C-V* methods can be explained in terms of the spatial distribution of the states based on the DIGS model.

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