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Fabrication of Less Than a 10nm Wide Polycrystalline Silicon Nano Wire

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This paper reports a fabrication technology of polycrystalline silicon (poly-Si) "slit nano wire", with dimensions of less than 10 nm. The processing procedures consist of a 100 nm electron beam lithography, precision dry etching, conformable deposition of silicon dioxide layer, slit etching, conformable deposition of doped amorphous silicon layer and etch back. The resulting poly-Si "slit nano wire" layer measures less than 10 nm in width as ascertained by a cross section transmission electron microscope (X-TEM). A possible application of the "slit nano wire" to a future optoelectronic devices is also discussed.

1. Introduction

Advances of silicon integrated circuit technology is limited to further microminiaturization beyond the 0.1 μm technology level [1], and several candidates for higher performance nano scale switching devices have been proposed. Quantum devices [2] are the most promising candidates to supersede silicon LSI's, however most activity has been focused on compound semiconductors and very few attempts have been made to fabricate silicon nano wire structures except for gate-controlled quantum inversion layers [3] and oxidation thinned silicon columns [4]. A silicon nano wire would make it possible to realize light emitting silicon by carrier injection, which would also make it possible to produce high performance optoelectronic integrated circuits. This paper aims to demonstrate silicon "slit nano wire" fabrication technology using 100 nm lithography combined with microwave etching and conformable deposition of silicon dioxide to confine the width and height of the trench.

2. Fabrication procedures of "slit nano wire"

The fabrication procedures of the "slit nano wire" is schematically shown in Fig. 1(A) through Fig. 1 (F). About 100 nm wide and 100 nm deep trenches were formed by fine beam electron beam lithography and microwave plasma etching in the silicon substrate (A). Then SiO_2 layer was conformably deposited to a thickness of about 50 nm, by a high temperature low pressure chemical vapor deposition (HLD), followed by a slight etching of SiO_2 in diluted HF acid (slit etch back) (B). Doped amorphous silicon (a-Si) layer was deposited by low pressure chemical vapor deposition (LPCVD). The phosphorus concentration was about 1 x 10^{20} cm^{-3} (C). The a-Si layer was etched back by microwave etching, and "slit nano wire" was successfully formed in the bottom of the slit (D). The sample was then annealed at 1000°C for 10 min to fully activate the doped phosphorus atoms and to crystallize the a-Si layer. Finally, a passivation layer was deposited (E), and the final "slit nano wire" structure is shown in (F).

The structures of the "slit nano wire" were observed by scanning electron microscope (SEM) and transmission electron microscope (TEM). The samples were cleaved and the cross sectional structures were observed by SEM after immersing the sample in a etching solution to delineate the outline of trenches and nano wire structures, if necessary. The conventional cross section TEM micrograph technology was utilized in observing the structures by TEM.

The advantage of the processing technology is that it enables the compatible fabrication of nano wire structures with conventional silicon LSI's. Therefore, integrated optoelectronic LSI's would be made possible if high efficiency light emission is achieved.

3. Results and discussions

The cross section SEM micrograph of the trench structure after silicon etching indicates that the fine beam electron lithography exposure and microwave etching successfully produced trenches in the silicon substrate approximately 100 nm deep and 100 nm wide. The SEM micrograph of the cross sectional structure after HLD SiO_2 deposition and "slit etch back" is shown in Fig. 2. The conformable coverage of the HLD SiO_2 layer over the trench is clearly depicted, and it is also demonstrated that the irregularities of the sidewall structure of silicon trench are relatively flattened.

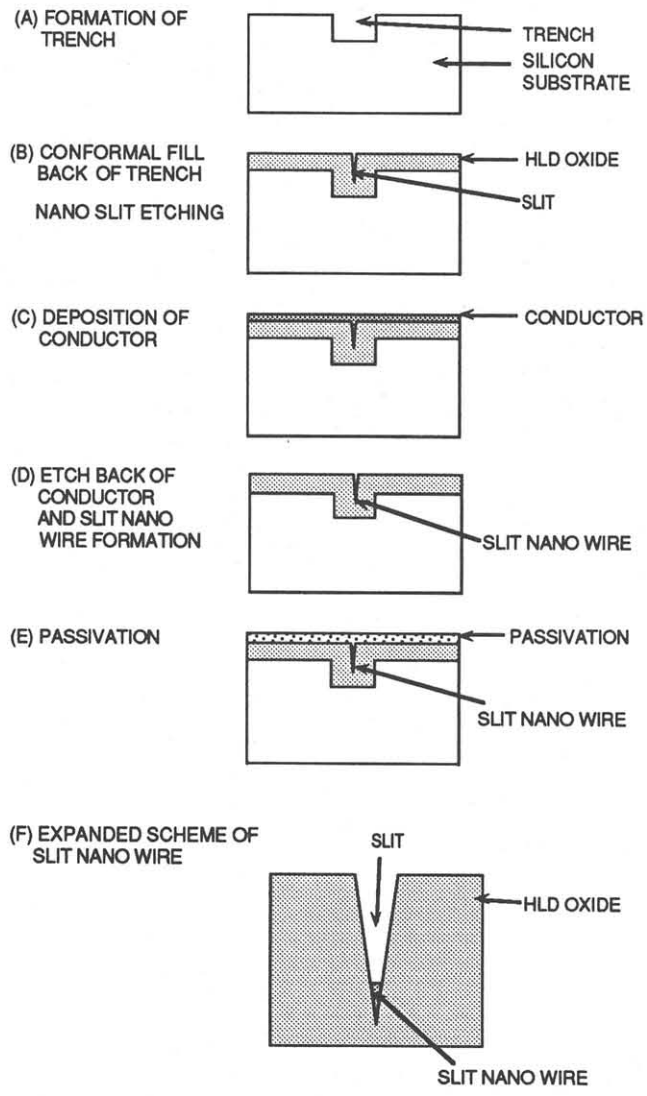

Fig. 1 Schematic presentation of "slit nano wire" fabrication process

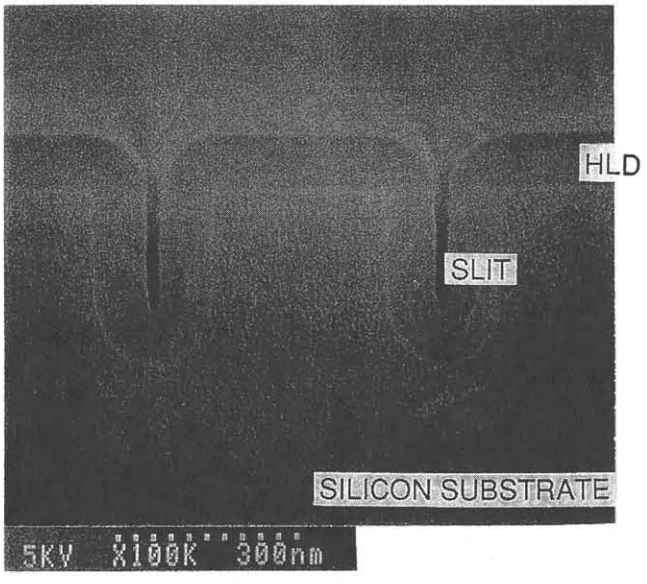

Fig. 2 SEM micrograph of the cross sectional structure after HLD SiO_2 deposition and "slit etch back"

The etching time dependence of remaining thickness of the a-Si layer from the bottom of the slit is depicted in Fig. 3. It is shown that the etching rate gradually decreases when a-Si layers are etched into the trench region and aspect ratio is increased. This etching depth dependence of etching rate can be attributed to the aspect ratio dependence of etching rate, as reported in [5], and the final a-Si layer might be removed very slowly and would leave a-Si "slit nano wire" in a self-aligned manner. This phenomenon is also one of the advantages of the "slit nano wire" process, in which the height of poly-Si layer can be controlled spontaneously.

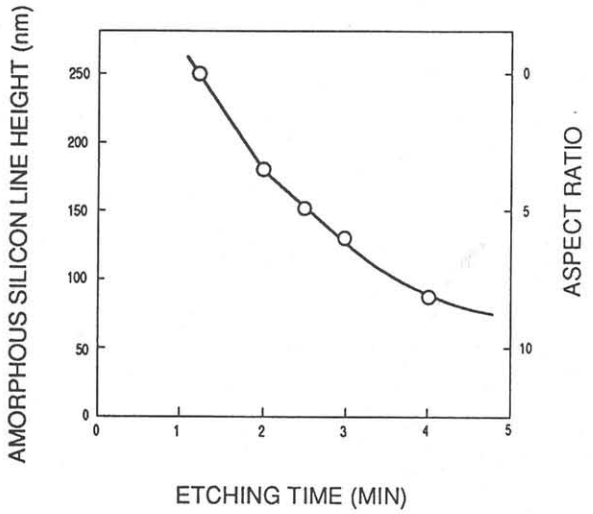

Fig. 3 Etching time dependence of the remaining doped a-Si layer thickness : etching rate decreases with the increase of aspect ratio

Cross section TEM micrographs of the polycrystalline silicon (poly-Si) "slit nano wire" embedded in the SiO_2 layer is shown in Figs. 4 (A) and (B). The lattice image TEM micrograph in (B) shows that the width of the nano wire is around 5-8 nm, while the height is around 20 nm. These dimensions might be slightly larger than the theoretically predicted dimensions to observe quantum effects due to volume confinement [5], though experiments to ascertain the quantum confinement effects are underway. The plan view TEM micrographs depicting the grain structure is shown in Fig. 5, in which the sample was annealed at 1000 C for 10 min., and the grain size is relatively small due to the rapid nucleation velocity at high temperatures [7]. Single crystal silicon nano wire structure would be preferable in applying to the optoelectronic devices. Therefore, low temperature, long time annealing of "slit nano wire" structure is more suitable for device applications. Experimental results indicate that the grains grew to a size of around 2 μm in the samples annealed at 540 C for 40 hours [8].

4. Conclusions

Polycrystalline silicon "slit nano wire" fabrication technology was presented, which would make it possible to realize less than a 10 nm wire structures. The silicon quantum devices as well as integrated optoelectronic circuits would be made possible by this technology.

Acknowledgments

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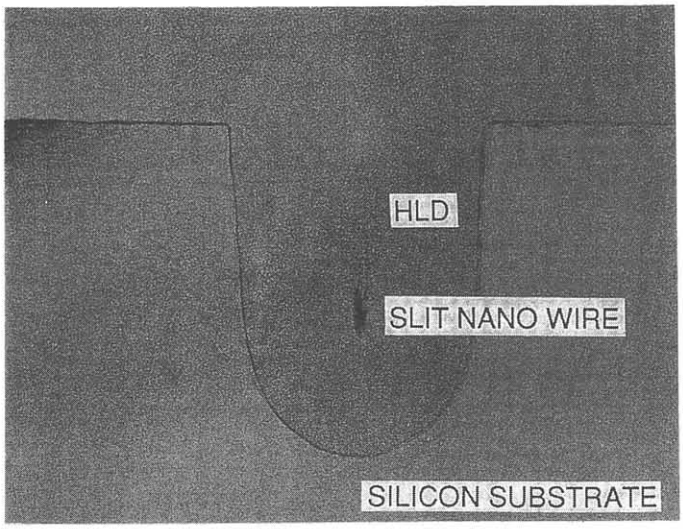

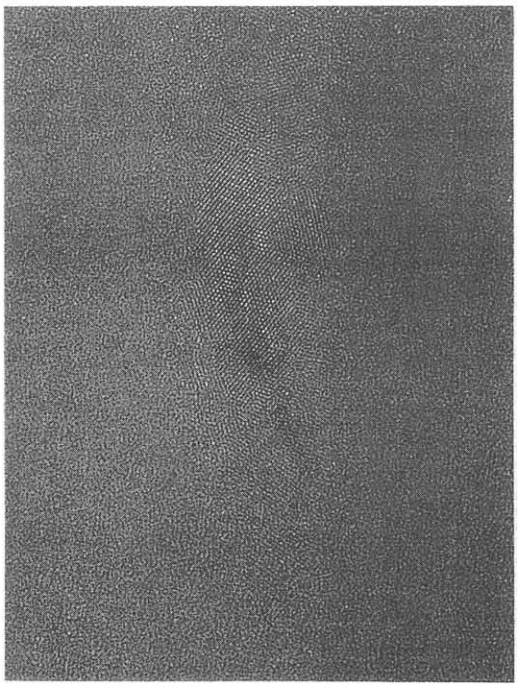

Fig. 4 Cross section TEM micrographs of the polycrystalline silicon "slit nano wire" embedded in the SiO_2 layer

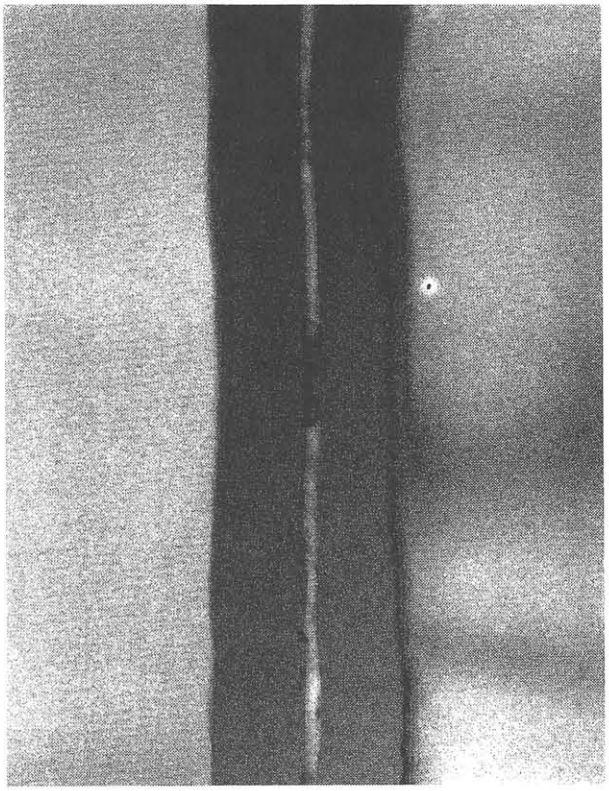

Fig. 5 Plan view TEM micrograph depicting the grain structure of the "slit nano wire" annealed at 1000 C for 10 min.

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