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Silicon MBE on Hydrogen Plasma Cleaned Substrates

E. Hammerl, W. Hansch, W. Kiunke, I. Eisele, J. Ramm*, E. Beck*

Institut für Physik, Fakultät Elektrotechnik
Universität der Bundeswehr München, D-85577 Neubiberg, FRG
*Balzers Ltd., FI-9496 Balzers, Liechtenstein

A hydrogen plasma was created with a UHV compatible plasma source. This low energy plasma was used to remove -in a single step- the native oxide and organic contamination from the wafer surface at low substrate temperatures (≤400°C). The cleaning process was applied to patterned substrates with micro shadow masks. Local epitaxial growth by MBE on these substrates was used to fabricate Triangular Barrier Diodes to demonstrate the device quality. The electrical results on these diodes are in agreement with the grown layer sequence and the chosen dopings.

Introduction

Molecular Beam Epitaxy (MBE) in silicon is well-suited for a defined vertical growth on an atomic scale. Additionally, in advanced semiconductor technology the lateral dimensions of patterned substrates are in the submicron range.
Perfectly cleaned and damage-free surfaces are necessary for the growth of device quality epitaxial layers. Different cleaning recipes have been investigated. Widely used is a chemical cleaning process [1] outside the growth chamber, followed by a high temperature (~900°C) desorption step in the ultra-high-vacuum (UHV) deposition chamber immidiately before the growth process. The problems connected with wet cleaning are the remove of nanoparticles and the penetration of the solutions into small openings like deep trenches. The high temperature step causes the destruction of very thin layers by diffusion or formation of alloys.
These problems can be solved by an in-situ plasma cleaning with hydrogen. Encouraging results have been obtained using different kinds of hydrogen plasma or hydrogen excitation to remove the native oxide and carbon contaminations from the silicon wafer surface [2,3]. These cleaning promises advantages over wet chemical cleaning, because they are compatible with in-situ processing and meet demands for an UHV production environment. Moreover, they could prove to play a decisive role in cleaning deep trenches and lowering the thermal budget during wafer processing for epitaxial growth. With plasma processes one has to take care to surface damage and roughness on an atomic scale, the incorporation of gas ions and the activation and contamination of atoms of the surrounding materials.

Experimental

The described processes were performed in an Modular UHV Multichamber System (MUM) [4] of Balzers Ltd. for 5"-wafers. We use three chambers for cleaning, deposition of isolators and silicides, and epitaxial silicon/germanium with doping, fed by two load locks containing 50 wafers.
The new Balzers plasma source is used for the hydrogen cleaning, which is described in greater details elsewhere [5]. This DC discharge generates high electron currents up to 100 A at low voltages (~25 eV) through the whole growth chamber, which acts as anode on ground potential. The electron energies are sufficient to dissociate the hydrogen molecules, but too low to cause substrate damage. The cleaning is believed to be pure chemical etching. We determined the etch rates for thermally grown SiO_2, diamond-like carbon and silicon, which can be controlled up to 1 atomic monolayer per second by the source parameters. Depending on the discharge parameters, the wafer surface can be prepared for epitaxial growth in the temperature range of 100° C to 400°C. No external heating for the substrate is used during hydrogen cleaning [6].
To demonstrate the device quality of this low temperature cleaning, specially in small openings, we used patterned substrates for local epitaxial growth of Triangular Barrier Diodes (TBD).
On (100)-n^+-substrates micro shadow masks

were fabricated. Details of this procedure are published recently [7]. The wafers were prepared by wet chemical cleaning [1], thermally oxidized (~1 µm) at 1050°C for 4 hours, followed by the deposition of a LPCVD nitride (100 nm in 45 min at T = 700°C with gas pressure of 0.3 mbar).
To define the structures of the desired openings common photolithography or electron-beam lithography was used. The etching of the Si_3N_4 top layer was performed by dry plasma etching in an CF_4/O_2-gas mixture in about 5 minutes. After remove of the resist the SiO_2 was etched in buffered hydrofluoric acid (BHF). The resulting micro shadow mask is shown in Fig. 1. The cleaned substrates were then loaded in the UHV system.

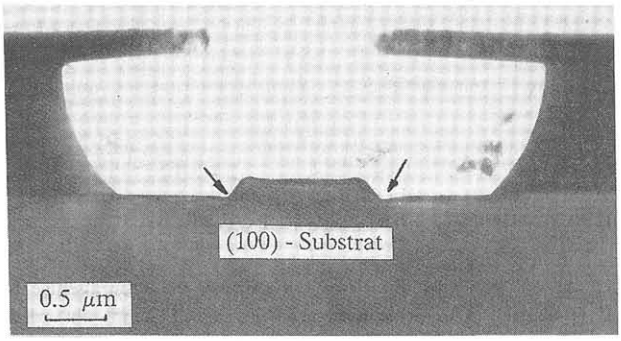

Fig. 1: Transmission electron micrograph of a local grown epitaxial silicon mesa after substrate cleaning by hydrogen plasma.

In the first chamber the described hydrogen plasma cleaning was performed. To show the effect of the etching process in the mask opening the source parameters were chosen to etch 50 nm of the silicon substrate in 5 min. The hydrogen pressure was about $2 \cdot 10^{-3}$ mbar, beam current 30 A with the beam 10 cm parallel beneath the substrate.
After the cleaning the wafers were transfered through the internal transport channel into the silicon growth chamber. Without a high temperature desorption step the deposition of the silicon layers was done. Between two 120 nm thick undoped silicon layers a 5 nm thick boron doped ($N_A = 1 \cdot 10^{18}\,cm^{-3}$) layer was formed. On top of this structure a degenerated ($N_D = 6 \cdot 10^{20}\,cm^{-3}$) antimony doped contact layer was grown. The p-type boron as well as the n-type antimony doping has been achieved by coevaporation out of effusion-cells at a substrate temperature of 470°C. To avoid unintentional doping of the intrinsic layers these layers have been grown at 700°C. At that temperature the incorporation of antimony is less than $5 \cdot 10^{16}\,cm^{-3}$, which is the detection limit of the SIMS measurement.
This layer sequence leeds to a triangular barrier in the banddiagram for electrons.
After the deposition the micro shadow masks were removed by an ex-situ lift-off process in hydrofluoric acid.
The electrical measurements were carried out on a common I(V)-equipment with an Hewlett-Packard 4145 B Parameter-Analyzer. The top contact was done by a needle, the backside contact was achieved by eutectical bonding of the n^+-substrate.

Results

Fig. 1 and Fig. 2 show transmission electron micrographs of plasma cleaned and local grown mesa structures. The etching of the substrate beneath the mask opening is clearly visible in Fig. 2.

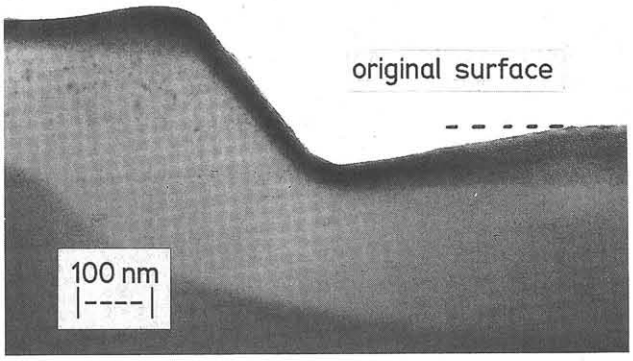

Fig. 2: Details on the side-wall of Fig. 1 as indicated by arrows.

The prepared surface for deposition can be recognized as a weak dark line at the bottom of the grown silicon mesa. This minor interface contaminations originate from the recontamination of the substrate during evacuation of the cleaning chamber after the plasma processing and the transport to the growth chamber (~15 min). None of the possible plasma damages are visible in the TEM investigations. The interface is smooth on an atomic scale, no bubbles of incorporated hydrogen or argon are detectable. The crystal quality of the epitaxial grown silicon is excellent without any defects.
This fact is confirmed by the electrical measurements of the fabricated TBDs. The diode characteristic at room temperature is shown in Fig. 3.
The diode shows a symmetrical characteristic. The threshold voltage $U_{th} = 0.44$ V is in agreement with the theoretical value of the chosen doping structure. An ideality factor of n = 2.13 can be calculated from the log(I)-V-characteristic. Mainly the parasitic current via the not passivated vertical mesa side-walls causes the difference to the theoretical value n = 2 of a symmetrical TBD. The reverse current density is about $1 \cdot 10^{-12}\,A/\mu m^2$.

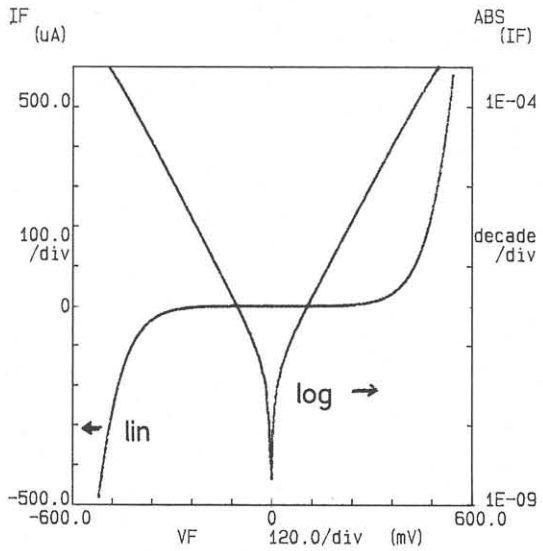

Fig. 3: I-V characteristics of a TBD grown on a hydrogen plasma cleaned substrate.

Conclusion

The plasma cleaning procedure presented is suited for UHV in-situ processing at low temperatures. The plasma ions and electrons have low energies which prevents damage to the crystalline silicon substrates. It is also shown that the cleaning procedure is suited for the preparation of patterned substrates for local epitaxial growth.
The electrical results of locally grown TBDs demonstrate the device quality of the cleaning process.
The combination of in-situ, low-energy and low-temperature plasma cleaning with low temperature growth processes allows the fabrication of complexe devices on a submicron scale for future devices.

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