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High-Mobility p-Channel MOSFET on Strained Si

D. K. Nayak[1], J. C. S. Woo, J. S. Park, K. L. Wang, and K. P. MacWilliams[2]

Department of Electrical Engineering
University of California, Los Angeles, CA 90024, USA
[2]The Aerospace Corporation, El Segundo, CA 90009, USA
[1]Present address : Research Center for Advanced Science and Technology (RCAST)
The University of Tokyo, 4-6-1 Komaba, Tokyo 153, Japan

An enhancement-mode high-mobility p-channel MOSFET is fabricated on strained Si layer for the first time. A biaxially strained pseudomorphic thin Si layer is epitaxially grown on a relaxed GeSi buffer on Si substrate by MBE. MOSFETs are fabricated using conventional Si process technology. It is found that low-field channel mobility of PMOSFET on strained Si is 50% higher than that of PMOSFET on bulk Si.

1. INTRODUCTION

Speed of Si VLSI circuit is steadily increasing by scaling the device dimensions. As device dimensions shrink to deep submicron regime, device scaling is becoming difficult. New materials and device structures are being sought to further improve the speed of future VLSI circuits on Si. It has been proposed that forming channel in a strained GeSi layer can enhance channel mobility of Si MOSFET devices [1]. This improvement in channel mobility comes from two factors, (i) reduction of carrier scattering at the SiO_2/Si interface, and (ii) higher in-plane hole mobility of biaxially strained GeSi [2-4]. High in-plane mobility results due mainly to the reduction of interband scattering of carriers in the valence bands, where band-edge degeneracy is lifted by strain. These GeSi PMOSFETs are buried channel devices and become surface channel devices at higher magnitude of gate bias. Then, the performance becomes comparable to surface channel Si device. In this work, we propose to fabricate PMOSFET on strained Si. This device, however, acts like a conventional surface-channel Si PMOSFET at higher magnitude of gate bias, which is important for circuit current drive. As the strained-Si has higher in-plane hole mobility than that of bulk Si, this surface-channel PMOSFET on strained-Si has higher channel mobility compared to that of surface-channel bulk Si PMOSFET.

Recently, Welser et al have shown a high-mobility NMOS on strained Si, but have found no performance improvement for PMOS on strained Si [5]. In this work, we demonstrate for the first time a high-mobility PMOS on strained Si which shows 50% higher channel mobility compared to an identically processed bulk Si device. Biaxial tensile strain in Si lifts degeneracy between light and heavy holes, and the spin-orbit band is lowered in energy [6,7]. Improvement in low-field in-plane hole mobility of strained Si results mainly from the reduction in interband scattering among light, heavy and spin-orbit bands [8].

2. SIMULATION

Device operation is explained using an 1-D device simulator. At small magnitude of gate bias, holes at the strained-Si/GeSi-buffer interface dominate channel conduction (Fig. 1). This device acts like a buried channel device. Channel mobility is expected to improved only due to reduced SiO_2/Si interface scattering as the in-plane hole mobility of the relaxed buffer is similar to that of bulk Si [9]. At high magnitude of gate bias, however, holes at the SiO_2/strained-Si interface dominate conduction (Fig. 2). The devices behaves like a surface-channel bulk Si device. But the channel mobility of this device is expected to be higher than that of bulk Si device because of the high in-plane hole mobility of strained-Si layer.

3. FABRICATION

The starting material consists of 1 Ω-cm, n-type, (001) Si substrate, 1 μm thick $Ge_{0.25}Si_{0.75}$ buffer layer, and 130 Å strained Si layer (by MBE at 550°C and doped n-type to 10^{16} cm^{-3}). PMOSFETs on strained Si and on bulk Si are fabricated using conventional Si process (65 Å gate oxide by RTO [10]). Drain, source and gate poly were doped p-type by B+ ($2X10^{15}$ cm^{-2} at 10 KeV). Implant annealing was done in two steps, (i) 550 °C for 1 hour, and (ii) 850 °C for 30 s. Al was used for metal contacts.

4. RESULTS AND DISCUSSION

I-V characteristics of long-channel Si (Fig. 3) and strained-Si (Fig. 4) PMOSFETs show good saturation and cut-off characteristics. Threshold voltages were -0.6 and -1.0V for strained-Si and Si devices, respectively. Strained-Si MOSFET shows higher current drive compared to bulk Si device. Saturation drain currents are 147 mA ($|V_g - V_t|$=1.4V) for strained Si device and 128 mA ($|V_g - V_t|$ = 1.5V) for bulk Si device.

Performance advantages of the strained Si device can be seen from linear transconductance measurement (Fig. 5). At a gate voltage close to threshold, holes are mostly confined at strained-Si/GeSi-buffer interface (Fig.1). In-plane hole mobility of an unstrained $Ge_{0.25}Si_{0.75}$ alloy layer is about the same as that of bulk Si. Therefore, channel mobility is low, and is comparable to that of bulk Si device (94 $cm^2/V.s$). At a higher gate overdrive ($|V_g - V_t| > 0.5V$), however, the device behaves like a surface-channel bulk Si device (Fig. 2). At $|V_g - V_t| = 1.4V$, the improvement in transconductance (channel mobility) is 50%. Also, the peak value of linear transconductance occurs at a much higher gate overdrive ($|V_g - V_t| = 0.84V$) than bulk Si. Improvements in linear transconductance (channel mobility) and current drive for a long-channel device show that in-plane hole mobility of strained Si layer is higher than that of bulk Si.

Comparable subthreshold slopes (108 and 111 mV/decade for strained-Si and Si, respectively) shows that the quality of the strained Si epilayer remains good after MBE growth and high-temperature processing (Fig. 6). Short-channel devices show good I-V and subthreshold characteristics (112mV/decade) (Fig. 7). The strain effect can be clearly observed even for short-channel (1.3 μm) devices (Fig. 7). The linear transconductance curve exhibits a broad peak with gate voltage, which signifies that strain induced enhancement is also present for short-channel devices, as discussed earlier in Fig. 5. A saturation transconductance of 41 mS/mm was measured at V_{ds}=-2V for the strained-Si PMOSFET (Fig. 8).

5. SUMMARY

In summary, we have demonstrated for the first time a PMOS on strained Si which exhibits higher current drive compared to that of a bulk Si PMOS. Channel mobility of a strained-Si device has been shown to be 50% higher than that of a similarly processed bulk Si device

6. ACKNOWLEDGEMENT

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7. REFERENCES

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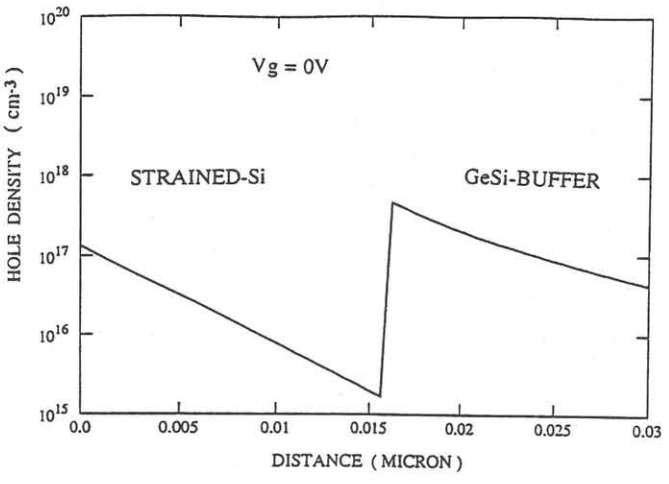

Fig. 1 : 1-D simulation of hole distribution for a gate voltage, V_g=0V.

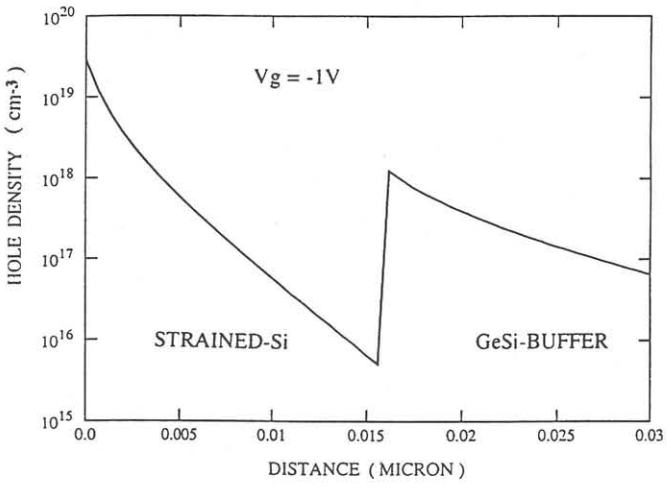

Fig. 2 : 1-D simulation of hole distribution for a gate voltage, V_g=-1V.

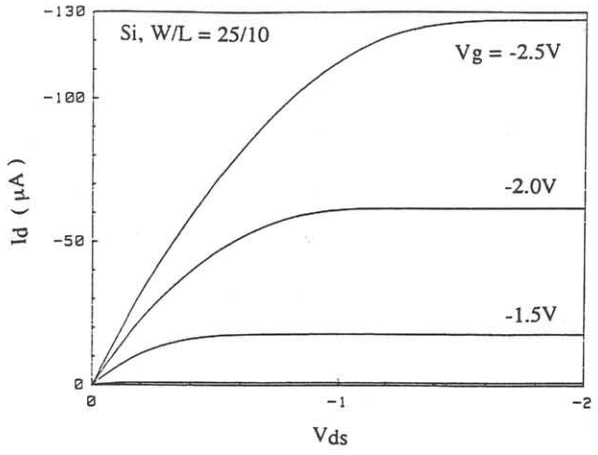

Fig. 3 : I-V characteristics of a long-channel bulk Si device (W/L=25/10).

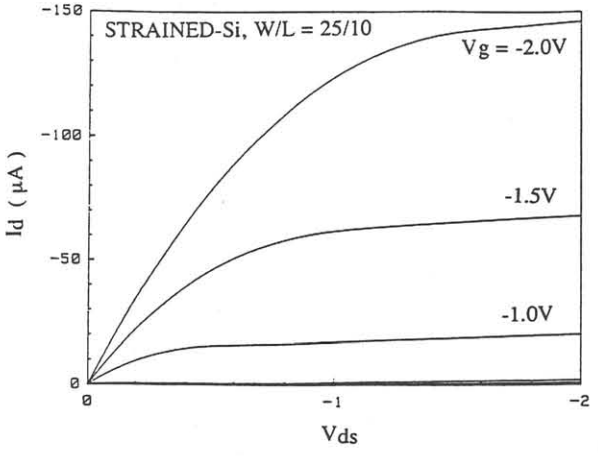

Fig. 4 : I-V characteristics of a long-channel strained-Si device (W/L=25/10).

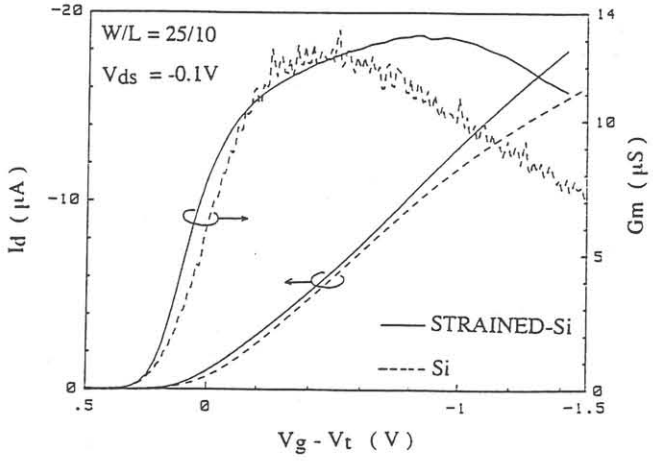

Fig. 5 : Comparison of drain current and linear transconductance for long-channel Si and strained-Si devices (W/L=25/10).

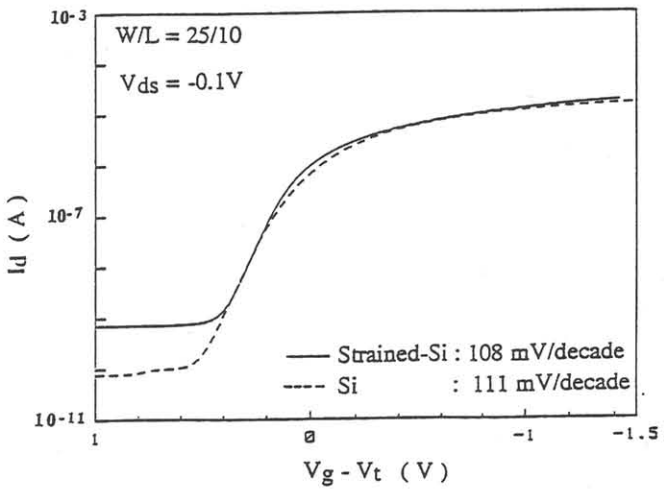

Fig. 6 : Comparison of subthreshold slopes of long-channel Si and strained-Si devices (W/L=25/10).

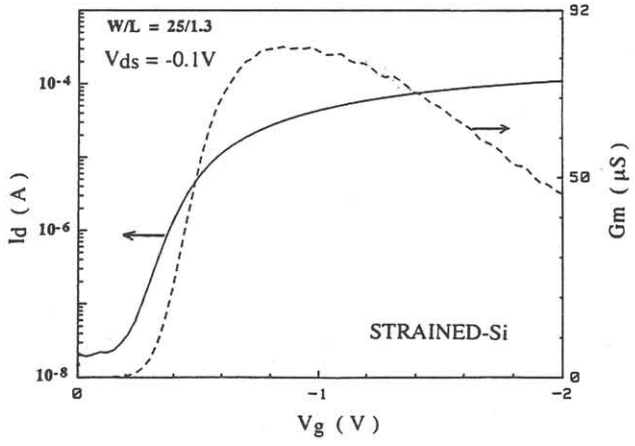

Fig. 7 : Linear transconductance and subthreshold slope of a short-channel strained-Si device (W/L=25/1.3).

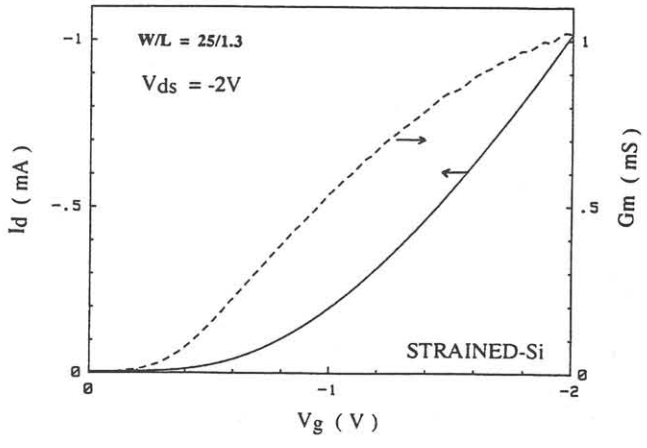

Fig. 8 : Saturation transconductance (V_{ds}=-2V) and drain current of a short-channel strained-Si device (W/L=25/1.3).