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Hole Confinement in a Si/GeSi/Si Quantum Well on SIMOX

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Si on insulator (SOI) technology is becoming important due to its potential use in future very large scale integration (VLSI) circuits. It has been proposed recently that GeSi PMOSFETs, which use Si/GeSi/Si quantum well as the channel, can offer performance leverage over conventional SIMOX PMOSFETs. In this work, hole confinement in a Si/GeSi/Si channel, which is grown by MBE on a SIMOX substrate, is investigated using device simulation and experimental techniques. Hole confinement is clearly demonstrated from experiment, which is found to be in good agreement with device simulation.

1. INTRODUCTION

Fully-depleted SOI MOSFETs show performance advantage over conventional MOSFETs on Si because of improved device isolation, reduced parasitic capacitance, and higher current drive. These properties have been exploited in fabrication of high speed SOI VLSI circuits [1]. On the other hand, GeSi PMOSFETs have been demonstrated to have higher channel mobility and current drive compared to conventional PMOSFET on Si [2-5]. This is achieved by confining holes of a pchannel device to a buried Si/GeSi/Si quantum well. This device, however, becomes a surface channel device at a higher magnitude of gate bias [6,7]. In this case, it behaves like a surface channel Si device due to large band bending at the Si surface. This surface band bending can be reduced significantly by using a SIMOX substrate instead of a bulk Si substrate [8,9]. This property has been used recently to fabricate highperformance GeSi-SIMOX PMOSFETs [8]. These GeSi MOSFETs on SIMOX show great promise for use in future VLSI circuits.

Fabrication of GeSi-SIMOX PMOSFETs requires growth of pseudomorphic Si/GeSi/Si heterostructure on SIMOX [8]. However, growth of a high-quality Si/GeSi/Si structure on SIMOX may be hindered by the presence of residual defects (dislocations, contaminants, etc.) in SIMOX. The goal of this work is to demonstrate hole confinement in a MBE-grown Si/GeSi/Si quantum well on a commercially available SIMOX using four different techniques, (i) Computer simulation, (ii) Capacitance-Voltage measurement, (iii) Linear transconductance measurement of GeSi SIMOX PMOSFET, and (iv) Channel mobility measurement of GeSi SIMOX PMOSFET using split C-V technique.

2. SIMULATION

C-V measurement can be employed to observe hole confinement in a MOS-gated Si/GeSi/Si structure, where a plateau in the inversion capacitance signifies hole confinement [6,7]. Using an 1-D device simulator, the hole confinements in a SiO₂ (65 Å)/Si (70 Å)/Ge0.3Si0.7 (100 Å)/Si structure on bulk Si and on SIMOX are obtained (Fig.1). Top 70Å of Si cap layer separates buried GeSi channel from Si/SiO2 interface, which results in diminished surface scattering of carrier in the GeSi channel. The plateau in the inversion capacitance of the structure on SIMOX is more pronounced and extends for a wider range of gate voltage (1.5V) when compared to that of the structure on bulk Si (1.1V). This implies improved hole confinement for the structure on SIMOX compared to that on bulk Si. It can be also seen from device simulation that the parasitic surface channel (conduction via Si cap layer) is suppressed by using SIMOX substrate instead of bulk Si [8].

3. C-V MEASUREMENT

Conventional SIMOX and GeSi SIMOX PMOSFETs are fabricated using a Si process [8]. Capacitance between gate and drain (drain and source tied together) of a 25μ mX25 μ m GeSi SIMOX PMOSFET (SiO₂ (65 Å)/Si (70 Å)/Ge_{0.3}Si_{0.7} (100 Å)/Si) shows plateau in inversion capacitance at 5KHz and 10KHz (Figs. 2 and 3). Hole confinement can be clearly observed by comparing capacitances between GeSi SIMOX and conventional SIMOX devices (Fig. 4). As can be seen in Fig. 4, threshold voltages for SIMOX and GeSi-SIMOX devices are -0.83 and -0.19V, respectively. This occurs due to the presence of unintentional doping during initial stage of epitaxial growth. In Fig. 5, the effect of this unintentional Boron (B) doping on inversion region capacitance is presented. The doping concentration has been calculated from the experimental shift of threshold voltages (Fig. 4). From Fig. 5, it is clear that buried GeSi channel dominates the inversion region capacitance when compared to that due to Boron doping.

4. GeSi-SIMOX PMOS MEASUREMENT

Hole confinement can also be observed from linear transconductance (Gm) measurement. The conventional SIMOX device shows a well defined peak, whereas for the GeSi SIMOX device $(25\mu m/10\mu m)$ Gm value remains at its peak value for a wide range of gate voltage (1.4V) (Fig. 6). This is because holes are mainly confined to the quantum well, the mobility of the GeSi layer is high, and the SiO₂/Si interface scattering is low. Hole confinement from this measurement (1.4V) agrees well with the simulation result (1.5V).

Assuming that all the holes are confined to the quantum well near threshold (which is verified from simulation), an effective gate capacitance (65 Å of SiO₂ in series with a 70 Å of Si cap layer) can be calculated. Using this effective gate capacitance, we obtain effective channel mobility from linear drain current measurement to be 182 cm²/V.s. Using a split C-V technique [10], which requires no information on gate capacitance, we measure effective mobility to be 184 cm²/V.s. Good agreement between these mobility values, which are obtained from two independent methods, further confirms hole confinement in the Si/GeSi/Si channel.



Fig. 1 : Device simulation results for GeSi-bulk Si and GeSi-SIMOX devices.

5. SUMMARY

In summary, using four different techniques we demonstrate hole confinement in a $Si/Ge_{0.3}Si_{0.7}/Si$ quantum well on SIMOX at room temperature for the first time. This opens up new opportunities in fabrication of GeSi/Si based heterostructure devices on SIMOX.

6. ACKNOWLEDGEMENT

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7. REFERENCES

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Fig. 2 : Measured capacitance at 5KHz of a GeSi SIMOX PMOSFET.



Fig. 3 : Measured capacitance at 10KHz of a GeSi SIMOX PMOSFET.



Fig. 4 : Measured capacitance at 10KHz of GeSi SIMOX and conventional SIMOX PMOSFETs.



Fig. 5 : Simulation resluts for inversion capacitances of (i) SIMOX, (ii) GeSi-SIMOX, and (iii) SIMOX with Boron doping.



Fig. 6 : Measured linear transconductance of a GeSi SIMOX PMOSFET.