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Invited

Silicon-on-Insulator for High Speed ULSI

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ABSTRACT

Bulk CMOS technology scaling can not sustain the historical rate of speed increase. A realistic target for SOI delay and power reductions are 40% and 30%, independent of scaling, mostly through capacitance reduction. Denser isolation allows more compact layout and easy integration of different high speed (E/D NMOS), low power (CMOS) and analog (bipolar, grounded-body CMOS) devices. Silicon device speed record (13 ps at 1.5V, 300K) has been set with SOI E/D NMOS. Leakage current due to steady state and transient floating-body induced threshold lowering (FITL) is a difficult device issue.

The Trend of Bulk Silicon Technology Scaling

The importance of electronics in the economic, social and even political development throughout the world will all but guarantee continued rises in circuit integration density and speed. It is less clear if bulk silicon technology can meet the historical trend of speed improvement. A recent study suggests that the speed trend can not be sustained [1]. I_{dsat} per unit channel width ceases to increase with technology scaling beyond the 0.5μm technology. Even when we examine the high-speed scenario, where Vcc reduction is delayed as much as reliability consideration might allow [1], I_{dsat} still ceases to increase. The unpleasant consequence on circuit speed is shown in (Fig. 1). Instead of the historical speed doubling every two generations, designers will need to work with speed doubling every four generations.

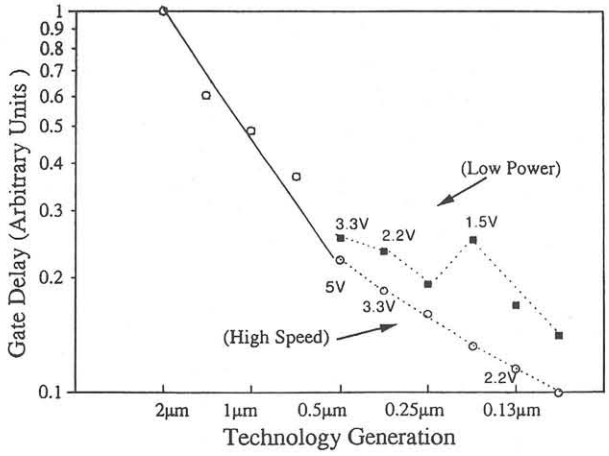

Fig.1. Bulk CMOS scaling can not sustain the rate of speed doubling every 2 generation beyond 0.35μm technology [1].

Capacitance Reduction with SOI

The most often cited advantage of SOI technology is higher speed due to reduction of junction capacitance because of the buried oxide. Comparison of bulk and SOI circuit power consumption provides the most direct data [2]. The ratio of power, $P = f \cdot C \cdot V_{dd}^2$, is equal to the ratio of circuit capacitance. Both data and calculations shown in (Fig. 2) suggest that SOI circuits have approximately two third the capacitance of bulk circuits.

		C (SOI)	C (bulk)	C (SOI) / C (bulk)
Active Gate (F.O.=1)	C_{OX}	36.6 fF	37.6 fF	0.97
N+ Junction (1 drain)	$C_{J(N)}$	9.5 fF	18.9 fF	0.50
P+ Junction (1 drain)	$C_{J(P)}$	7.6 fF	21.6 fF	0.35
Polysilicon (10 μm^2)	C_{POLY}	0.43 fF	0.98 fF	0.44
1st Aluminum (1mm)	C_{1AL}	72.6 fF	123.2 fF	0.59
2nd Aluminum (1mm)	C_{2AL}	63.9 fF	98.4 fF	0.65

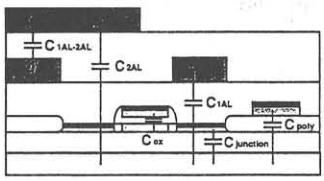

Fig. 2. Comparison of circuit power consumption has confirmed that typical circuit capacitance is reduced to $^2/_3$ of the bulk circuit. Buried oxide is 500nm thick [2].

We expect this capacitance advantage to remain relatively constant independent of scaling. Buried oxide needs to be "electrically" thicker than or physically as thick as the depletion region under the source/drain.

Subthreshold Current and Floating-body Induced Threshold Lowering (FITL)

There are three components of MOSFET leakage current [1]. One is bulk leakage often referred to as punchthrough. SOI eliminates this leakage path easily. The second component is a surface leakage component known as drain-induced barrier lowering, V_T lowering, or short channel effect, $I_d(V_g=0) \propto 10^{-V_t/S}$ SOI offers an opportunity to bring S close to the limit of 2.3kT or 60mV/decade through the use of fully-depleted thin-film SOI [3]. Unfortunately, as V_{ds} increases, drain-body junction leakage and gate-induced drain leakage [4] cause holes (in the case of NMOSFET) to flow into the floating body. This raises the body potential and hence lowers V_T and increases the leakage (Fig. 3) independent of channel length. This can happen even when the silicon film is fully depleted. This floating-body induced leakage is a very serious and difficult problem, especially when one considers transient V_T drift.

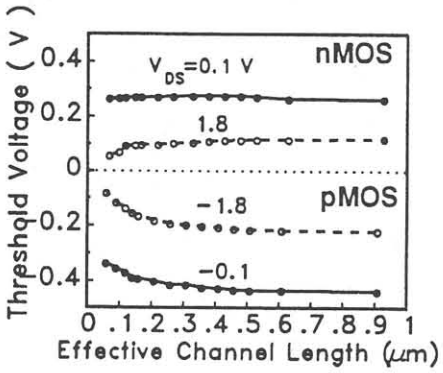

Fig. 3. Floating-body induced threshold lowering (FITL) lowers V_T and raises subthreshold leakage at high V_{ds} even in long-channel devices. Gate oxide is 4.2nm [5].

There are several potential solutions — raise V_T to allow a margin, provide a contact to the body, or make body/source "leaky". We believe there is an important device design concept — use light body doping so that there is minimal potential variation across the silicon film thickness. This "uniform barrier" design will minimize the barrier against hole flow into the source for a given barrier against electron flow into the channel (the subthreshold current).

Enhanced MOSFET Current?

Although reports on SOI devices typically show lower I_{dsat} than bulk devices of the same oxide and channel dimensions, SOI MOSFET can potentially produce larger I_{dsat} than bulk device as shown in (Fig. 4) [6].

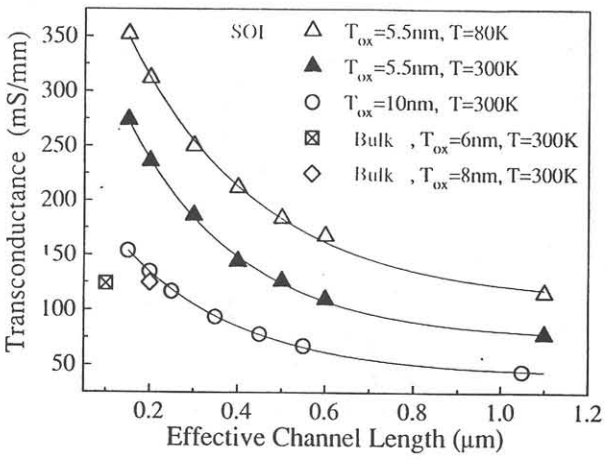

Fig. 4. SOI MOSFET can provide larger current than bulk devices due to reduction in V_T and bulk charge is S/D resistance is not excessive. The 5.5nm gate SOI PMOSFETs produced the highest tranconductance ever reported [6].

The most important reason for SOI's larger I_{dsat} in future low V_{dd} operation is the possibility of lower V_T [1] — if floating-body induced V_T lowering can be controlled. Otherwise, FITL still leads to an effective reduction in V_{Te} of about 0.15V at high V_{ds} and enhanced I_{dsat} in steady state [6]. Finally, reduced bulk charge effect [7] can increase I_{dsat} by around 10% [6] if the buried oxide is effectively much thicker than the bulk depletion region thickness. On the other hand self heating and thin SOI's higher S/D resistance reduce I_{dsat}.

Overall, we expect about the same I_{dsat} in SOI and bulk MOSFET's, with about 10% advantage toward SOI especially at very low V_{dd}, with thicker buried oxide and salicided S/D.

Reliability and Technology Issues

In spite of high dislocation density and metal impurity concentrations, SIMOX as well as bonded SOI materials appear to be capable of producing bulk quality gate oxide [8]. Hot carrier reliability is compromised due to charge trapping in the buried oxide. However effective graded LDD can be produced without trade-off with junction depth. Adequate hot electron reliability is predicted.

More than speed, leakage and reliability issues. Manufacturability will likely decide SOI's future. In this respect, SOI has several advantages in isolations, latch-up, shallow junction, contact formation, layout density, etc. It is worth noting that there are novel and intriguing SOI material and device ideas. One example would produce dense, vertical double-gated thin SOI devices using a bulk silicon substrate as the starting material [9].

Conclusion and Discussion

A critical review suggests that bulk technology scaling can not sustain the historical rate of speed increase. SOI reduces circuit capacitance by 30%, and

can potentially increase MOSFET current by 10% through reduction in V_T and bulk change. Ease of device isolation allows SOI technology to integrate CMOS, complementary BJT, E/D NMOS [10], high voltage device and analog MOSFETs with body contacts. Fastest silicon circuit delay record has been set with SOI E/D NMOS (13 ps at 1.5V and 300K) [11] (Fig. 5). Highest PMOSFET transconductance record has been set with SOI technology (Fig. 4). Manufacturability advantages may favor SOI as the main-stream technology beyond the 0.15 μm technology. Moderately thin (limited by S/D resistance) fully depleted SOI on moderately thick (limited by self heating) buried oxide is the most attractive arrangement. "Uniform barrier" design is proposed to minimize floating-body induced threshold lowering (FITL).

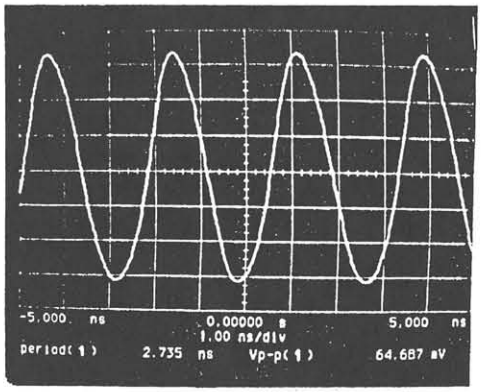

Fig. 5. Fastest silicon transistor speed record, 13ps, has been set with E/D NMOS on SOI technology. 101 inverter ring oscillator, V_{dd}=1.5V, T_{ox}=7nm, T_{si}=50nm, $Leff \approx 0.15\mu m$, 300K [11].

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