Extended Abstracts of the 1993 International Conference on Solid State Devices and Materials, Makuhari, 1993, pp. 143-145

Hot-Carrier Related Phenomenon in MOSFETs with Furnace N_2O-Nitrided Gate Oxides

G. W. Yoon, J. Ahn, G. Q. Lo, and D. L. Kwong

Microelectronics Research Center
The University of Texas at Austin, Austin, TX 78712

In this paper, the hot-carrier related reliability issues in both n- and p-MOSFETs with furnace N_2O-nitrided gate oxides have been investigated under application specific stress conditions such as for SRAM-type pass transistors, CMOS logic-circuit transmission gates and CMOS analog devices. Excellent hot-carrier immunity against various stress environments has been demonstrated, suggesting that N_2O-nitrided gate oxides are promising for numerous MOS ULSI applications.

1. INTRODUCTION

Recent studies show that MOSFETs with furnace N_2O-grown gate oxides have enhanced current drivability and reliability [1]. Through the self-limiting N_2O-oxidation mechanism, one can have excellent thickness control in *ultrathin* range (≤60 Å). However, for thicker (>80 Å) gate oxide formation using N_2O oxidation, a much larger thermal budget is required. More recently, we have developed a novel and flexible gate dielectric fabrication technique based on furnace nitridation of thin thermal SiO_2 in pure N_2O ambient to produce high quality gate dielectrics with *desirable thickness for specific applications* [2]. Improved device characteristics with N_2O-nitrided gate oxides have been demonstrated.

This paper addresses hot-carrier related reliability issues in both n- and p-MOSFETs with furnace N_2O-nitrided gate oxides under application specific stress conditions such as for SRAM-type pass transistors, CMOS logic-circuit transmission gates and CMOS analog devices. Our results show that all the hot-carrier induced damages (*i.e.*, interface states, electron/hole trapping and neutral electron traps) are greatly suppressed in N_2O-nitrided gate oxides, and excellent hot-carrier immunity against various stress environments has been demonstrated. These results suggest that furnace N_2O-nitrided gate oxides are promising for numerous MOS ULSI applications.

2. EXPERIMENTAL

Conventional n- and p-MOSFETs (W_{eff}/L_{eff}=15 μm/0.8-15 μm) were fabricated using CMOS twin-well technology with LOCOS isolation. Control oxide (~85 Å) was grown in pure O_2 at 950°C, followed by a 950°C, 15 min N_2 anneal. N_2O-nitrided oxide (~85 Å) was prepared by first growing SiO_2 (~50 Å) in pure O_2 at 850°C, followed by N_2O-nitridation at 950°C which grew additional ~35 Å oxide. $[N]_{int}$ at SiO_2/Si interface was ~1.5% as measured by AES. The thicknesses were measured by both ellipsometer and *C-V* measurements. No channel V_t-adjustment implant was performed, thus both n- and p-MOSFETs are surface channel devices.

3. RESULTS AND DISCUSSION

Fig. 1 shows TDDB characteristics of MOS capacitors with control and N_2O-nitrided gate oxides under substrate electron injection. Capacitors with N_2O-nitrided gate oxides have much tighter t_{BD} distribution and larger t_{BD} value. In addition, n-MOSFETs with N_2O-nitrided oxides show less charge trapping and interface state generation (ΔD_{it}) under DC hot carrier stress (not shwon).

Device reliability under AC-stress was investigated. $\Delta g_m/g_{m,0}$ has been studied under DC-stress with alternating hot-carrier injection modes with a fixed high V_d. For control devices, $\Delta g_m/g_{m,0}$ is enhanced during high V_g-stress (*i.e.*, electron-injection) after each low V_g stress (*i.e.*, hole-injection). The enhanced degradation is believed to be due to neutral electron trap generation [3]. Since the enhancement in $\Delta g_m/g_{m,0}$ (after each cycle) is smaller in N_2O-nitrided oxide devices compared to control devices, it can be concluded that the neutral electron trap generation is much suppressed for N_2O-nitrided oxides. Since the neutral electron traps are believed to be generated through the recombination of injected electrons with trapped holes [4], the suppressed neutral electron trap generation in N_2O-nitrided oxides could be partially due to the reduced hole trapping.

The reduced neutral electron trap generation provides N_2O-nitrided oxide device an enhanced hot-carrier immunity against AC-stress such as for SRAM-type pass transistors operating under a fixed high V_d with AC-

pulsed V_g in high frequency. Under AC-stress, enhanced degradation compared to that under DC-stress is observed in both devices due to neutral electron trap generation. Since the neutral electron trap generation is significantly suppressed in N_2O-nitrided oxide, the enhancement is significantly less than control devices. The AC-stress enhanced degradation should not be due to ΔD_{it} since no enhanced I_{sub} was observed during AC-stress (under proper S/D grounding and long τ_r/τ_f). As a result of the suppressed neutral electron trap generation, the AC-stress induced degradation in N_2O-nitrided oxide device has much weaker dependences on pulse frequency and duty-cycle compared to control devices (Fig. 2). Therefore, N_2O-nitrided oxide devices are very suitable for SRAM-type pass transistors application with enhanced reliability.

Unlike n-MOSFETs, p-MOSFETs with control and N_2O-nitrided SiO_2 gate show no enhanced degradation under alternating stress phases. This is because that the injected hole density at high V_g (with high V_d) is not large enough to induce neutral electron traps. As a result, no enhanced AC-induced degradation is observed for p-MOSFETs. However, because of reduced electron trapping in N_2O-nitrided oxides, p-MOSFETs with N_2O-nitrided oxides show an improved hot-carrier immunity over control oxide devices, as shown in Fig. 3.

Fig. 4 shows $\Delta g_m/g_{m,0}$ of p-MOSFETs under bi-directional stress. During forward stress, p-MOSFETs with N_2O-nitrided oxides show less $\Delta g_m/g_{m,0}$ than control devices due to reduced electron trapping. Under subsequent reverse stress, the lateral electric field increased drastically as a result of trapped electron-induced channel L_{eff}-shortening [5]. This resulted in a much enhanced electron injection and thus the suddenly enhanced $\Delta g_m/g_{m,0}$. Because N_2O-nitrided devices has much suppressed electron trapping during forward stress, $\Delta g_m/g_{m,0}$ due to reverse stress is significantly suppressed. The bi-directional stress in p-MOSFETs represents a worst-case scenario regarding p-MOS transmission gate transistors' reliability, since it aggravates the hot-electron induced punchthrough (HEIP) by shortening L_{eff} from both S/D. Therefore, for CMOS transmission gate application where S/D are switched alternatingly to high state, p-MOSFETs with N_2O-nitrided oxides are extremely suitable with greatly enhanced reliability over control devices.

The reliability of submicron CMOS analog devices was also investigated. For low V_d, because of the suppressed acceptor-type ΔD_{it} for N_2O-nitrided oxides [2, 6], r_o-degradation was reduced. For high V_d, smaller increase in r_o observed for N_2O-nitrided oxide device (than for control device) indicates that the donor-type ΔD_{it} was also suppressed in N_2O-nitrided oxides. Since N_2O-nitrided oxide devices have reduced Δg_m and Δr_o, voltage gain degradation $\Delta(g_m \cdot r_o)$ can be greatly suppressed, as shown in Fig. 5. In addition, device with N_2O-nitrided oxides also shows less decrease in V_{swing} than control devices.

Furthermore, n-channel N_2O-nitrided devices do not show any degradation of g_m or I_d at subthreshold and low V_g region whereas control oxide devices show a significant degradation (not shown). The non-degraded low V_g's characteristics make N_2O-nitrided device an excellent device matching stability for wide range of I_d against hot-carrier stress, as shown in Fig. 6(a). In comparison, control device shows a larger device mismatching (V_{offset}-degradation) at all I_d levels due to ΔD_{it}-induced carrier density loss (low I_d) and mobility degradation (high I_d).

For p-MOSFETs, the V_{offset}-degradation under hot-carrier stress is due to electron trapping induced ΔV_t. Because of the reduced electron trapping, the V_{offset}-degradation was also suppressed in device with N_2O-nitrided oxide compared to control device (Fig. 6(b)).

4. CONCLUSION

The hot-carrier related reliability issues have been studied in detail in both n- and p-MOSFETs with furnace N_2O-nitrided gate oxides under application specific stress conditions. Our results show that all the hot-carrier induced damages (*i.e.*, interface states, electron/hole trapping and neutral electron traps) are greatly suppressed in N_2O-nitrided gate oxides, and excellent hot-carrier immunity against various stress environments has been demonstrated. These results suggest that furnace N_2O-nitrided gate oxides are promising for numerous MOS ULSI applications.

This work was supported by SRC/SEMATECH and the Texas Advanced Technology Program

5. REFERENCES

1) W. Ting *et al.*, **EDL-12**, 1991, p. 416.
2) J. Ahn *et al.*, **EDL-13**, 1992, p. 494.
3) K. Mistry and B. Doyle, **EDL-11**, 1990, p. 267.
4) I. C. Chen *et al.*, *J. Appl. Phys.*, 1987, p. 4544.
5) M. Koyanagi *et al.*, in *IEDM Tech. Dig.*, 1987, p. 844.
6) J. E. Chung *et al.*, in *IEDM Tech. Dig.*, 1990, p. 553.

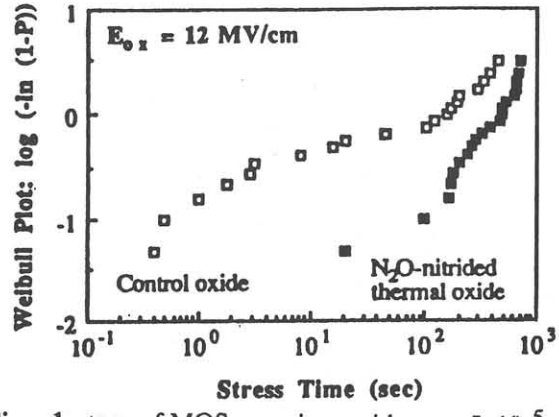

Fig. 1 t_{BD} of MOS capacitors with area=5×10^{-5} cm^2.

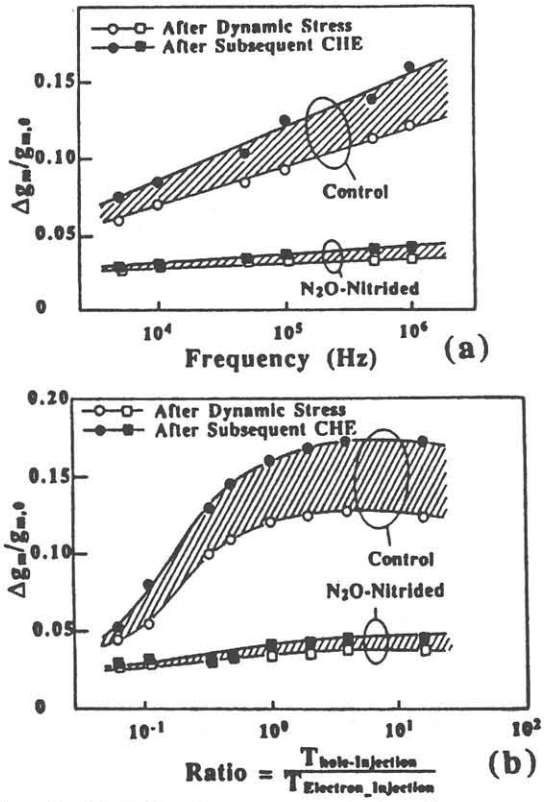

Fig. 2 (a) Pulse frequency and (b) h^+-injection period dependences of $\Delta g_m/g_{m,0}$ for n-MOSFETs under AC stress and subsequent CHE-injection.

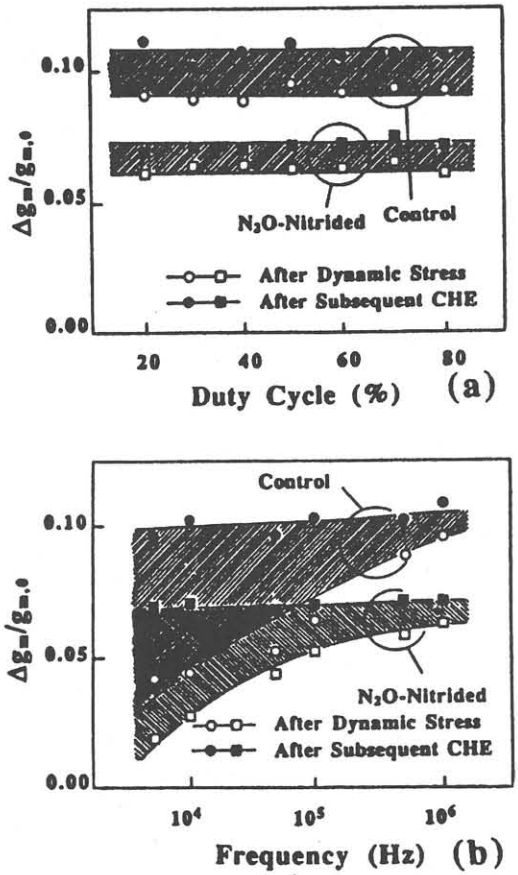

Fig. 3 (a) Pulse frequency and (b) h^+-injection period dependences of $\Delta g_m/g_{m,0}$ for p-MOSFETs under AC-stress and subsequent CHE-injection.

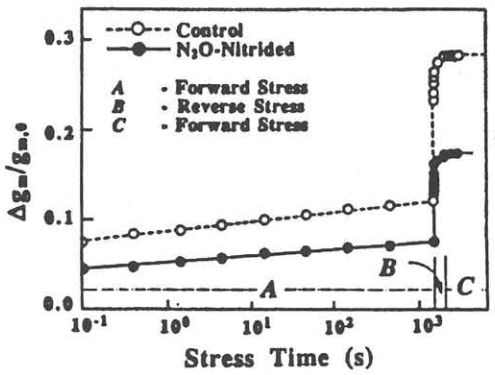

Fig. 4 $\Delta g_m/g_{m,0}$ in p-MOSFETs under bi-directional stress. S/D during reverse stress were interchanged from that during forward stress.

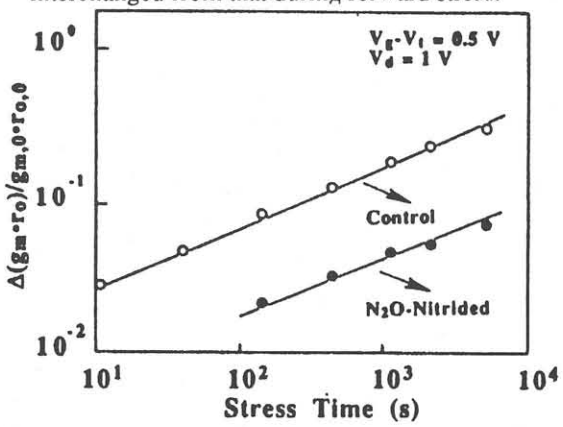

Fig. 5 $\Delta(g_m \cdot r_o)$ vs. stress time for n-MOSFETs.

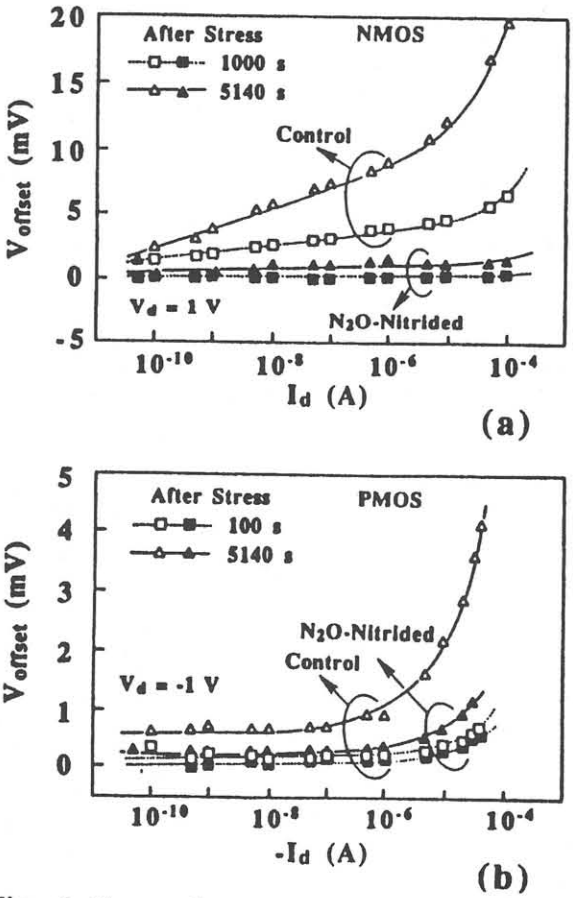

Fig. 6 V_{offset}-degradation in (a) n-MOSFETs and (b) p-MOSFETs.