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Influence of Si-SiO_2 Interface Microroughness and Dopant Concentration on Electron Channel Mobility in MOSFET

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The channel mobility in MOSFET is an important factor that determine the speed performance of devices. Miniaturization of device dimension requires high dopant concentration in substrate. In this paper, we have investigated the influence of the Si-SiO_2 interface microroughness and the dopant concentration of Si substrate on the electron channel mobility. As a result, the Si-SiO_2 interface microroughness strongly dominates the electron channel mobility in MOSFET as the inversion layer gets thinner together with higher dopant concentration.

1. INTRODUCTION

The channel mobility in MOSFET is one of the most crucial factors that determine speed performance for devices. Therefore, it is very important to maintain the channel mobility at a high level in order to realize high speed computer architecture. At the same time, miniaturization of device dimension for ULSI devices requires high dopant concentration in substrate in order to overcome the short-channel effects. However, employing a substrate with high dopant concentration results in lower carrier mobility[1]. The thin inversion layer of MOSFET caused by high dopant concentration is supposed to be one of the origins of the low carrier mobility. It is reported that the microroughness of the Si-SiO_2 interface degrades channel mobility by scattering carriers[2,3,4]. It can be easily speculated that the influence of the microroughness of the Si-SiO_2 interface on channel mobility is enhanced when the inversion layer becomes thinner. The purpose of this paper is to investigate the influence of the Si-SiO_2 interface microroughness and the dopant concentration on the electron channel mobility in MOSFETs. In order to understand the relationship between microroughness and dopant concentration, we introduced the $P\text{-}V/X_{inv}$ value, where peak-valley(P-V) height for Si-SiO_2 interface microroughness is divided by the inversion width(X_{inv}).

2. EXPERIMENTAL

In this experiment, Cz boron-doped p-type (100) wafers were used. For the purpose of evaluating the effect of dopant concentration, three types of wafers with different dopant concentration were used. The dopant concentration were 2.0×10^{16}, 2.1×10^{17}, and 2.5×10^{18}. The Si-SiO_2 interface microroughness was controlled by changing the NH_4OH mixing ratio in the $NH_4OH/H_2O_2/H_2O$(APM) solution of RCA cleaning before gate oxidation[4]. In this experiment, hot ultrapure water dipping (90°C, 10min) was carried out right after APM cleaning. In this sequence, NH_4OH in APM solution was introduced to the subsequent hot ultrapure water dipping vessel by adhering to the wafer and wafer cassette. The amount of introduced NH_4OH depends on the NH_4OH concentration in APM solution. The wafer surface was roughened by hot alkaline solution dipping because hot alkaline solution etches Si substrate rapidly and irregularly. The surface microroughness was measured by Atomic Force Microscopy (AFM), where the height accuracy is calibrated on the order of 0.1nm[5]. Then n-MOSFETs (n^+ poly silicon/SiO_2/p-Si(100), T_{ox}=9nm) were fabricated to evaluate the electrical characteristics. The dry oxidation was carried out in the ultraclean environment characterized by extremely low metal and airborne impurity concentrations to focus in the influence of microroughness and substrate characteristics[6].

3. RESULTS AND DISCUSSION

Figure 1 shows the relationship between the average surface microroughness(Ra) and NH_4OH content ratio in APM solution (dopant concentration = 10^{16}). The surface microroughness increases as the NH_4OH concentration gets higher. There was no statistical difference between the surface microroughness for the three different dopant concentration. It is believed that the surface microroughness formation by alkaline solution is independent of the dopant concentration in wafer substrate when it is less than 10^{18}. Figure 2 (a) and (b) show the AFM images of the silicon surfaces after APM cleaning. The dopant concentration of substrate is 2.0×10^{16}. The mixing ratio of APM solution is set at 0.05:1:5 in the case of (a) and 1:1:5 in the case of (b). The AFM profiles are considered to indicate the microroughness on the $Si-SiO_2$ interface at the channel area.

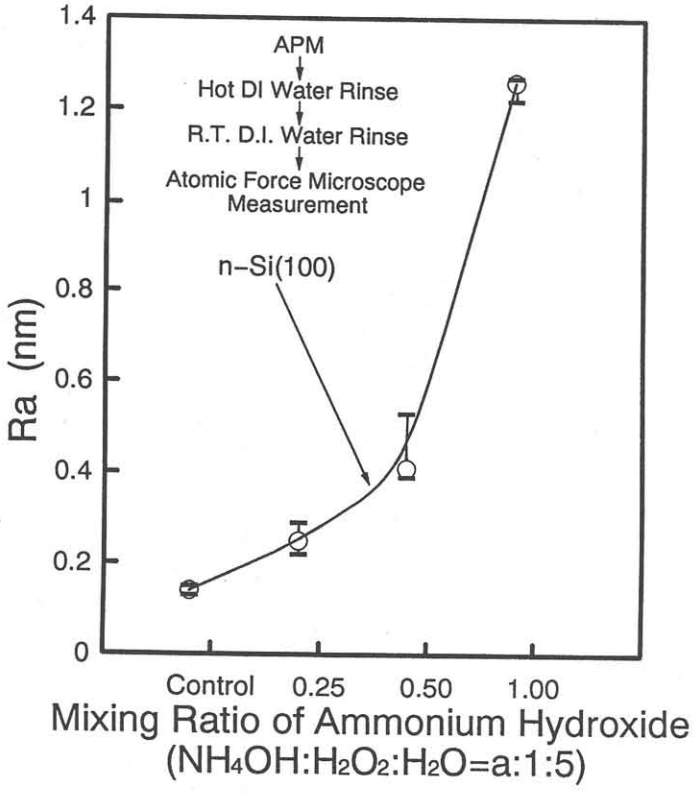

Figure 1 Relationship between average surface microroughness(Ra) and NH_4OH content ratio in APM solution.

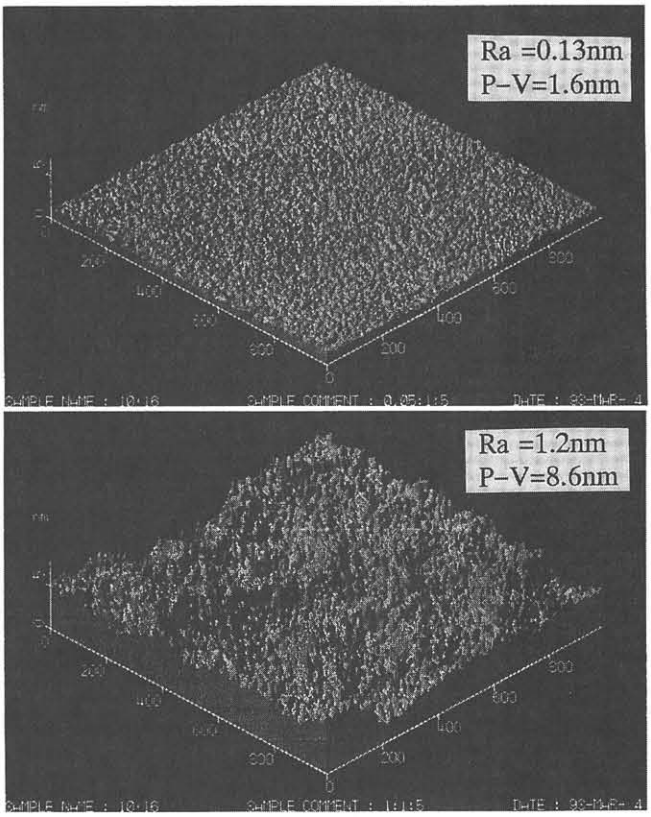

Figure 2 (a) and (b) AFM images of silicon surfaces after APM cleaning. Mixing ratio of APM solution is set at 0.05:1:5 in the case of (a) and 1:1:5 in the case of (b).

Figure 3 shows the influence of dopant concentration and $Si-SiO_2$ interface microroughness on electron channel mobility in n-MOSFET. Electron channel mobility (μ_n) was derived from I_D-V_G characteristics of n-MOSFET in saturation drain current region by the following equation.

$$I_D = \frac{W}{2L}\mu_n C_{ox}(V_G - V_{TH})^2$$

The degradation of electron channel mobility greatly depends on the increase of $Si-SiO_2$ interface microroughness, as the dopant concentration becomes higher. The origin of the larger degradation by the higher dopant concentration is considered to be its thinner inversion layer. In order to investigate the influence of the inversion layer, we introduced the value normalized peak-valley(P-V) height for $Si-SiO_2$ interface microroughness divided by the inversion width(X_{inv}). Figure 4 shows the relationship between the electron channel mobility and the $P-V/X_{inv}$ value. In the region where $P-V/X_{inv} \geq 0.3$, the electron channel mobility is strongly influenced by $Si-SiO_2$ interface

microroughness. From these results, it is believed that the carriers were mainly scattered by microroughness at the Si–SiO_2 interface and consequently obstructed the mobility. Since the inversion width reduces when the dopant concentration is high, the carrier scattering caused by the Si–SiO_2 interface microroughness becomes more pronounced.

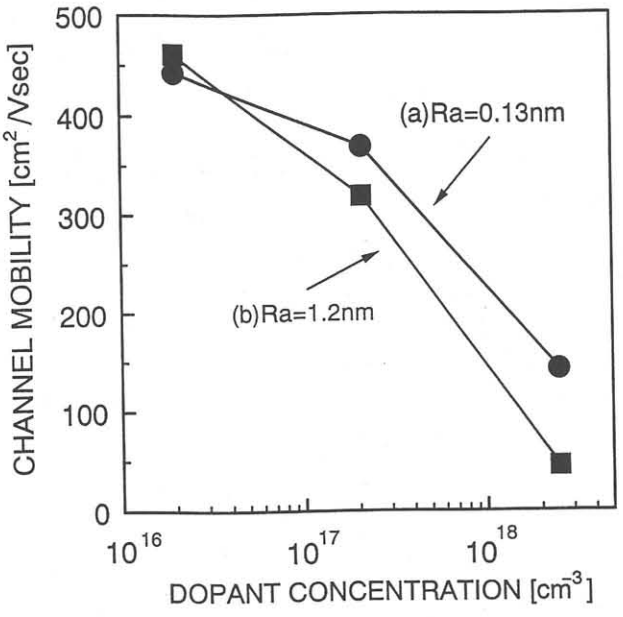

Figure 3 Electron channel mobility in n–MOSFET for dopant concentration and Si–SiO_2 interface microroughness. Electron channel mobility was derived from I_D–V_G characteristics of n–MOSFET in saturation region.

4. CONCLUSIONS

The influence of the Si–SiO_2 interface microroughness and the dopant concentration of Si substrate on the electron channel mobility was investigated. The Si–SiO_2 interface microroughness strongly dominates the electron channel mobility in MOSFET as the thickness of inversion layer gets narrow together with higher dopant concentration. Since substrates with higher dopant concentration are required for future miniaturized ULSI fabrication, it will become more important to improve the smoothness of the Si–SiO_2 interface in order to produce high speed ULSI circuits.

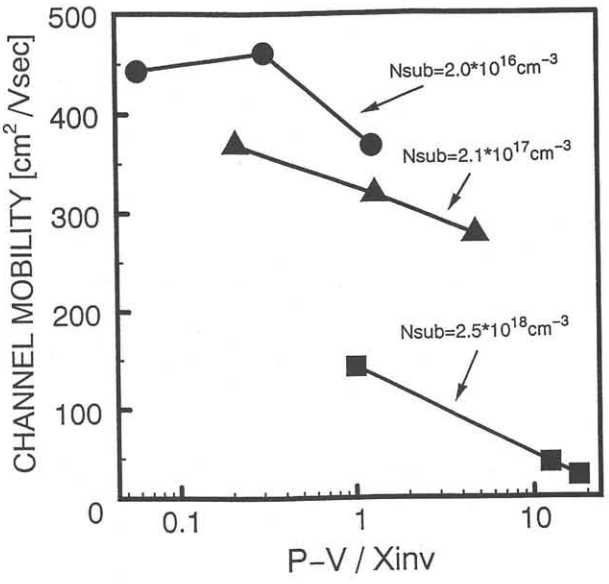

Figure 4 Relationship between electron channel mobility and the value normalized peak–valley(P–V) height for Si–SiO_2 interface microroughness divided by the inversion width(X_{inv}).

5. ACKNOWLEDGEMENT

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