Extended Abstracts of the 1993 International Conference on Solid State Devices and Materials, Makuhari, 1993, pp. 92-94

Invited

Spatially Resolved Characterization of the Si/SiO_2 System Using Conducting Atomic Force Microscopy

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We have combined the high spatial resolution and topographic imaging abilities of Atomic Force Microscopy with small area electrical measurements between a conducting cantilever and silica films on silicon. We observe applied fields before breakdown exceeding 30 MV/cm, and uniform dielectric properties of high quality oxide films. With defective dielectric films we observe correlations between the electronic properties of the film and topographic features. We have studied the individual electronic properties of sub micron MOS capacitors and also observed high field values prior to breakdown.

1) INTRODUCTION

The technique of Atomic Force Microscopy (AFM) is well suited to the topographic characterisation of surfaces on extremely small scale, having a spatial resolution of a few nm's and the ability to function on insulting substrates. By combining an AFM with a conducting cantilever and tip, we have been able measure electronic properties of insulating materials on a fine scale. In particular the conducting tip can emulate the metal plate of a Metal Oxide Silicon (MOS) Capacitor when scanned over a silica film on a silicon substrate. We have used this system to image the dielectric properties of silica films, and to study the properties of ultra-small capacitor structures.

2) EXPERIMENTAL

The principles of the Conducting AFM system and the data acquisition electronics and software have been described in detail elsewhere[1]. Briefly the system consists of a conventional AFM system equipped with an optical system to monitor cantilever deflection. In the experiments described here conducting silicon cantilevers were used[2], with contact forces of the order of 100 nN. The digital control electronics was extended to allow the generation of a bias voltage on the sample and the measurement of the synchronous current flowing between the sample substrate and tip. The bias is applied via a 10^8 Ω series resistance to limit the current flowing should a breakdown of the insulating layer occur.

3) RESULTS

Fig 1. shows a Current/Voltage (I/V) spectrum taken at a single point between the tip and a silicon substrate with 12 nm of device quality thermal oxide. Below an applied voltage of ~20 Volts no current can be measured and above this value a rapidly rising current, characteristic of Fowler-Nordheim (FN) conduction, may be observed.

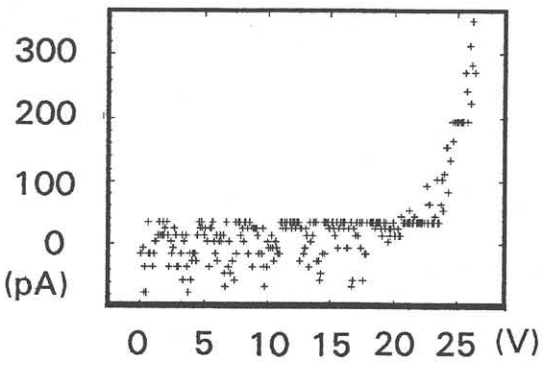

Fig 1. The Tip current (pA.) as a function of the Applied Sample Bias (V).

Analysis of the FN region shows good agreement between the expected work function and area of the emitting surface and those derived from the data[1]. Multiple I/V measurements from the same point appear identical until eventual breakdown of the dielectric is observed, showing the measurement to be essentially reproducible and the breakdown properties of the oxide to be history dependent, consistent with experience from conventional breakdown measurements of MOS structures[3].

The I/V curve obtained shows that we may clearly detect a FN current of ~50 pA in a dynamic measurement. The system has been applied to a number of oxide samples with different process histories. The technique developed is to ramp the sample bias at each image pixel until a pre-set current is detected, remove the bias, record the topography, current and bias values for the pixel and move the tip to the next imaging point. In this fashion an image may be constructed of the voltage required to generate a constant current across the dielectric.

In general, for high quality oxide films less than 10 nm thick, we consistently observe threshold voltages which correspond to applied fields in excess of 30 MV/cm. If the film has little topographic structure we find no observable structure in the threshold voltage images of the dielectric, over areas up to 20 microns. If the oxide is contaminated from process defects the defects appear as low voltage areas in the Voltage image and may usually be correlated with topographic feature in the AFM image.

Most recently we have used the conducting AFM to image sub-micron MOS capacitors, and make simultaneous electronic measurements of the individual devices. Fig 2 shows a topographic AFM image of a 10.4 micron scan across an array of capacitors approximately 0.5 microns in diameter. The devices were fabricated on 8.5 nm oxide films using a dry etching process. The metal layer consists of 50 nm of aluminium overlaying the oxide on each capacitor. The topographic image shows the height of each capacitor as greater than 100 nm, indicating that the etching process has completely removed the metal and oxide layers in-between the devices and etched into the silicon substrate. The distorted shape of the capacitor images is probably due to a convolution of the capacitor topography and the AFM tip.

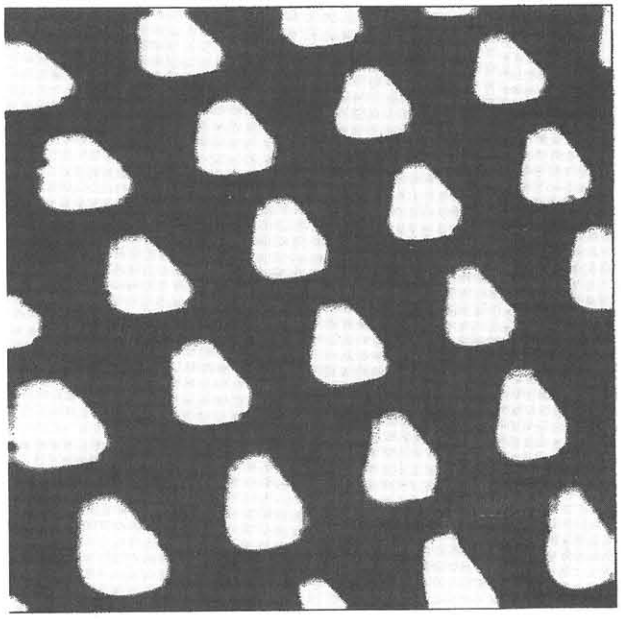

Fig 2. 10.4 micron AFM Topographic image. Vertical scale corresponds to 110 nm.

Initial electronic images of the capacitors revealed identical voltage maps across all capacitors imaged, however repeat scans revealed a progressive failure of the devices. Fig 2b) shows a threshold voltage image of the same area of capacitors, taken simultaneously with Fig 2a).

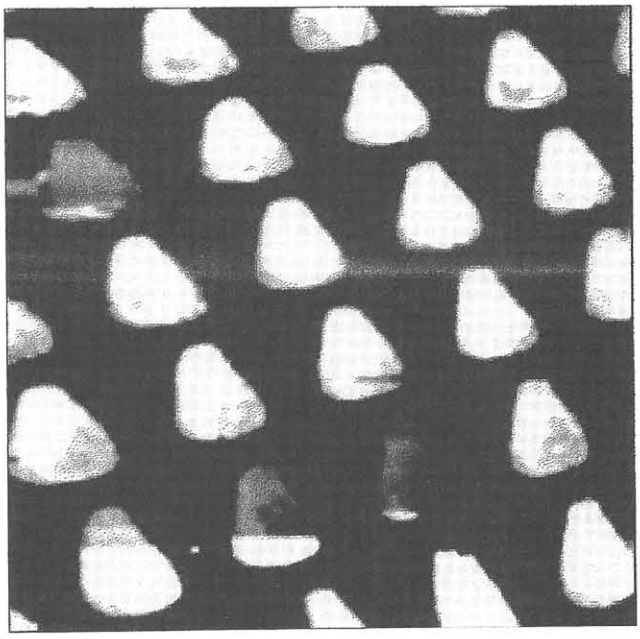

Fig 3 The threshold Voltage of the area in Fig 2. Whit to Black corresponds to 0-29.5 Volts The threshold current was 20 pA.

This image was the 5th identical repeat scan of the same area. The threshold current level was set at ~20 pA and each capacitor underwent approximately 250 voltage ramps per image. Whilst we observe the majority of the capacitors to be still capable of withstanding voltages of 30 V (Corresponding to an applied field of 35MV/cm), three of the devices have now failed as a result of repeated electronic stressing. Whilst these devices appear unchanged in the topographic image, the threshold voltage to develop a small current is now greatly reduced. The capacitors therefore appear considerably darker in Fig 3. than those remaining electronically intact. Continued imaging of the same area showed some 30% of the capacitors to remain intact after a further 3 scans.

4) DISCUSSION

The electronic images of the capacitors provides much useful information. Firstly, the area in-between the capacitors is uniformly dark, with a bias voltage of less than 0.2V. This shows the absence of any voltage offsets or artefacts due to series resistance which might explain the large observed fields on the capacitors. Once a capacitor has broken down it will conduct the threshold current at a uniformly low bias across the entire capacitor. Thus the electronic contact between the tip and metallisation layer provides a low resistance contact.

Such observations lead us to the conclusion that small area devices on ultra thin oxide films can withstand repeated extremely high bias without undergoing permanent breakdown.

5) CONCLUSION

We have shown that a conducting AFM tip may be used to emulate the metallisation of an MOS capacitor. The effective area of the MOS device may be as small as 20 nm in diameter. Electronic studies from such systems agree with conventional capacitor data, with the exception of the large fields apparently sustainable by the dielectric over such small areas. Scanning electronic measurements on high quality dielectric films do not indicate the presence of dielectric "weak areas" which might be responsible for the failure of larger area devices at conventional breakdown bias values of 13 MV/cm.

In addition the same technique has been used to make individual electronic measurements of sub-micron MOS devices and shows breakdown fields in excess of 35 MV/cm, with a distribution of the ability of the devices to withstand multiple stressing. To our knowledge this represents the first individual isolated electronic measurement of 0.5 micron devices and offers much promise as a technique for future measurement of both fundamental dielectric behaviour on small scales, and state-of-the-art device characterisation using electronic connections on a nanometre scale.

Preliminary studies have also shown the technique to be sensitive to the capacitive coupling between the substrate and tip. These studies may lead to highly localised Capacitance-Voltage (CV) measurements and the spatial mapping of interface states and trapped charge distributions.

The authors are indebted to M.Heyns, S. Verhaverbeke P Mertens and A. Rotondaro of IMEC, for developing the capacitor fabrication techniques. This work was supported by ESPRIT basic research actions PROMPT and ASSIST and funding from East Coast Scientific Ltd.

6) REFERENCES

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