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High Dielectric Constant Ferroelectric Thin Films for DRAM Applications

J. Lee, C. Sudhama, J. Kim, and R. Khamankar
Microelectronics Research Center
University of Texas, Austin, TX 78712

This paper describes the thickness scaling characteristics of ferroelectric lead zirconate titanate (PZT) thin films for gigabit DRAM storage capacitor applications. High-temperature (400°C) sputtering deposition technique demonstrates very high charge storage density (~ 37μC/cm^2 for 2V operation) with low leakage current density (~10^{-7}A/cm^2 at 2V) and good dielectric breakdown behavior. This technique also allows the desirable reduction of grain size of perovskite phase (<1000Å) and a scaling of thickness to less than 300Å while maintaining excellent dielectric integrity. A 650Å PZT thin film has an equivalent SiO_2 thickness of 1.9Å. In this paper, an accurate and simple technique to characterize the intrinsic discharge time for these thin films has been developed. The effects of lanthanum doping will also be discussed.

Ferroelectric materials such as PZT (lead zirconate titanate) have attracted a lot of attention recently because of their wide range of applications such as storage capacitor dielectrics for ultra-high density dynamic random access memories (DRAMs), nonvolatile ferroelectric memories, pyroelectric detectors, and integrated sensors and microactuators. The paper focuses on the application of the high dielectric constant properties of ferroelectrics to DRAM capacitor dielectrics [1-2]. Ferroelectric materials which have been reported to have dielectric constants as high as 10^4 [3], compared to dielectric constants of 3.9 for SiO_2 and ≈20 for Ta_2O_5 [4-5], hold good promise as an alternative to the conventional complicated trench and stacked capacitor cell structures in order to meet the charge storage density requirement of ULSI DRAMs.

$PbZr_{0.65}Ti_{0.35}O_3$ films with very fine grain size were prepared by DC-magnetron sputtering deposition from a multi-component Pb/Zr/Ti metal target in a pure oxygen ambient at 400°C, and subsequent annealing at various temperature in an N_2 ambient. Film thickness was scaled from 1000Å to 270Å and platinum has been used for both top and bottom electrodes. X-ray diffraction patterns show purely perovskite phase with no low dielectric constant pyrochlore phase. The range of interdiffusion between PZT and Pt is narrow (see AES depth profile in Fig. 1) which indicates a thinner interfacial layer; this avoids low-value series capacitance and leads to high charge storage density (for 650Å thick films). The grain size is typically less than 1000Å (Fig. 2), which should yield very uniform cell-to-cell characteristics on the gigabit DRAM chip where the cell area is expected to be reduced dramatically.

Charge storage density and leakage current density of 650Å films, deposited with 30W PZT target power and 9W Pb compensation for 2V DRAM operation are shown in Fig. 3 as a function of annealing temperature. As annealing temperature increases, leakage current density rises steeply, which may be due to enhancement of Pb vacancies [6]. Thus when leakage current density is taken into account, an annealing temperature of 550°C gives a film with optimum characteristics under 2V operation (Q'_c = 37μC/cm^2 and J_L= 4x10^{-7}A/cm^2). Time-dependent dielectric breakdown properties have been examined. Time-to-breakdown is extrapolated to greater than 10 years under 2V operation (Fig. 4).

Effective SiO_2 thickness is commonly used to compare the effectiveness of high-dielectric constant thin films (Fig. 5) [7-9]. An optimized low-temperature (200°C) sputter deposited 1000Å PZT film has an equivalent SiO_2 thickness of 4.7Å [7] while sol-gel derived PZT films of 700Å have been reported to have an equivalent SiO_2 thickness of 2.1Å for 0.75V operation [8]. A 1000Å BST ((Ba,Sr)TiO_3) film equivalent to 13Å of SiO_2 has been reported recently [9]. In comparison, an optimized 650Å thick sputtered PZT film deposited at 400°C is equivalent to 1.9Å of SiO_2, with a leakage current density of less than 4 x 10^{-7}A/cm^2 for 2V operation. Furthermore, the 270Å film exhibits a value close to that of the 650Å film. This implies that effective dielectric constant decreases as the film thickness is reduced. It is observed by AES that in the 270Å film there is severe depletion of Pb near the interface between PZT and the bottom Pt electrode; on the other hand, the Pb concentration is uniform throughout the 650Å PZT film. The anomalous interface in the 270Å film may act as a series capacitor and thereby reduce the effective dielectric constant. Even though scaling down the thickness to less than 300Å causes a reduction in dielectric constant, the charge storage density and leakage current density (less than 10^{-6}A/cm^2 at 2V) satisfy requirements of 256Mb DRAMs.

The conduction behavior for these thin films is important since it is related to the refresh time in DRAM operation. Refresh time is usually defined as the time taken for the ferroelectric capacitor to discharge to 80% of its initial value [8]. However, there are still questions regarding the accurate method of measuring leakage [10]. A simple technique has been developed to accurately characterize the intrinsic discharge time has been developed (Fig. 6). This involves the monitoring of the capacitor voltage under open circuit condition after a write operation. The intrinsic discharge time is found to decrease with increasing operating voltage (Fig. 7) and correlates quite well with the conventional leakage current measurement (Fig. 8).

Lanthanum dopant is commonly believed to increase resistivity and reduce the Curie temperature [11]. Sol-gel derived $PbZr_{0.5}Ti_{0.5}O_3$ thin films have been incorporated with 5-20 atomic % of lanthanum dopants. The results indicate that the charge storage density decreases with an increase in La concentration (Fig. 9). Furthermore, there appears to be an optimum La concentration at which the leakage current is minimum (Fig. 10). Leakage current increases with La concentration beyond 5%, which indicates that the increasing volatility of Pb overwhelms the effect of the enhanced La doping concentration, due to a departure from the equilibrium composition $Pb_{(1-1.5x)}La_xV_{x/2}(Zr_{.5}Ti_{0.5})O_3$ where V represents a Pb vacancy.

ACKNOWLEDGMENTS

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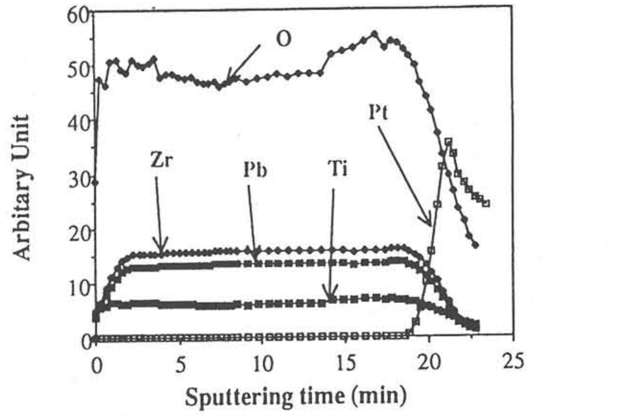

Fig. 1. AES depth profile of 650Å sputtered PZT thin film deposited at 400°C and annealed at 575°C. PZT and Pb target powers were 30W and 9W respectively.

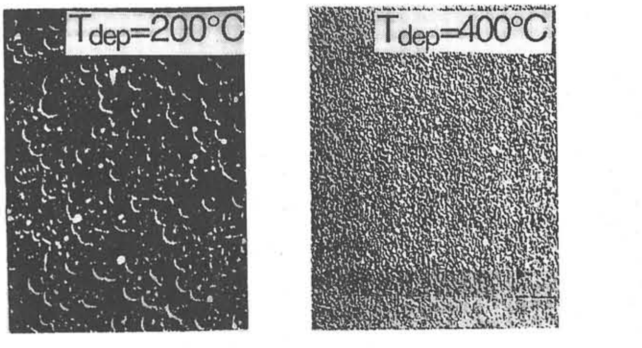

Fig. 2. Nomarski micrographs for 1000Å sputtered PZT deposited at (a) 200°C and (b) 400°C. Both were annealed at 575°C.

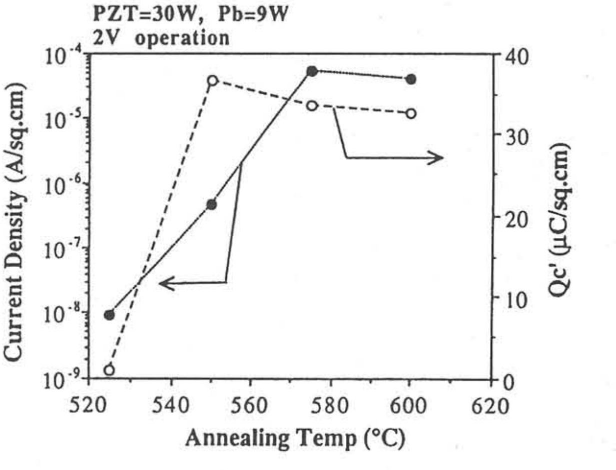

Fig. 3. Charge storage and leakage current density of 650Å PZT films for 2V operation, plotted as a function of annealing temperature. The films were sputter deposited at 400°C.

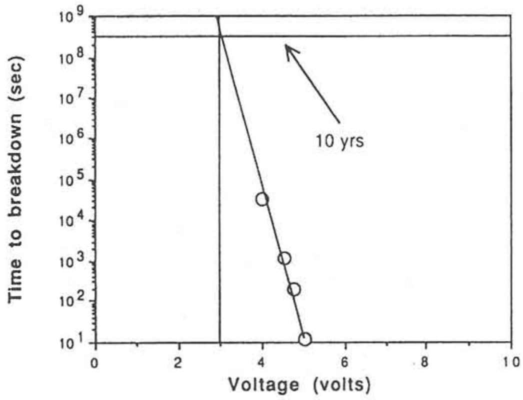

Fig. 4. Time-dependent dielectric breakdown behavior for 650Å thick PZT sputtered deposited thin films.

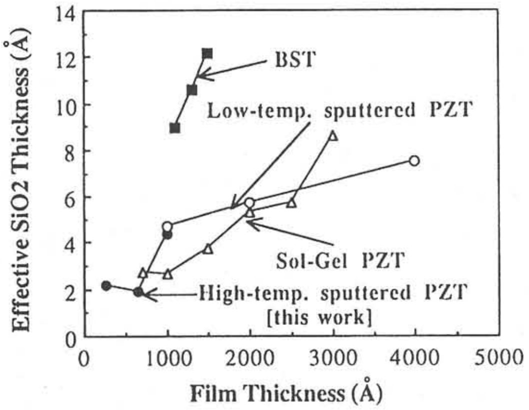

Fig. 5. Comparison of effective SiO_2 thickness as a function of dielectric film thickness for various deposition techniques and materials.

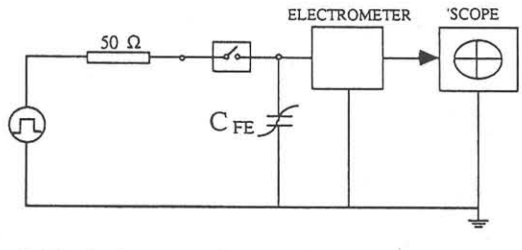

Fig. 6. Technique to characterize the intrinsic discharge time of ferroelectric thin films.

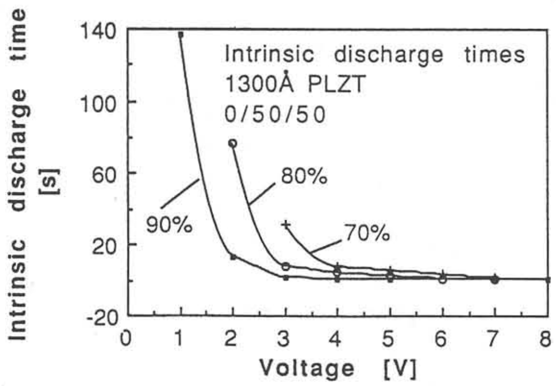

Fig. 7. Intrinsic discharge time vs. operating voltage as a function of refresh-time criteria (i.e. time taken to discharge to 90%, 80%, 70%).

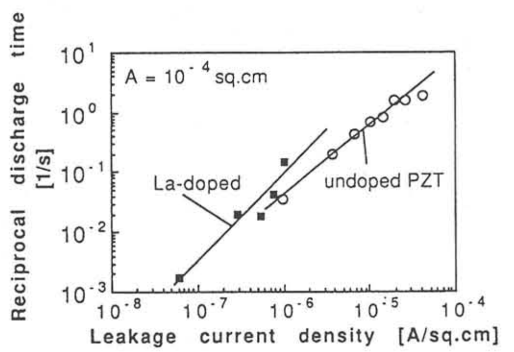

Fig. 8. Correlation of reciprocal of the intrinsic discharge time with leakage current density.

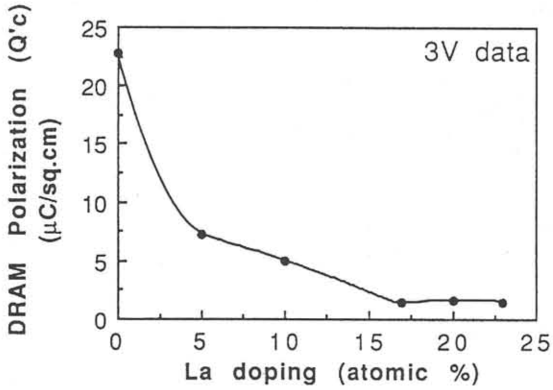

Fig. 9. The effects of lanthanum doping on charge storage density for DRAM applications.

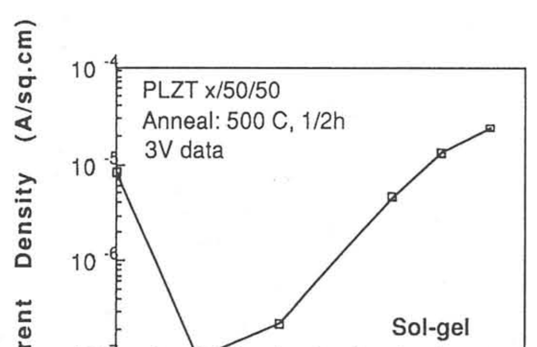

Fig. 10. Leakage current of PLZT films as a function of La atomic %. There exists a minimum in leakage current.